









# Index

1	Features of	Zeroplus Logic Analyzer	
	1.1 Раскаде Со	ontents	5
	1.2 Introduction	l	7
	1.3 Hardware S	specifications	9
	1.4 System Red	quirements	
_	1.5 Device Mai	ntenance and Safety	
2	Installation.		14
	2.1 Software In	stallation	
	2.2 Hardware Ir	nstallation	
_	2.3 Tips and Ad	lvice	
3	User Interfac	≫e	
	3.1 Menu & loc	l Bars	
	3.2 Find Data V	alue	
	3.3 Statistics Fe	eature	
	3.4 Customize	Interface	
	3.4.1 Modify	Waveform Display Mode	
	3.4.2 Modify	Ruler Mode	
	3.4.3 Modify	Waveform Height & Correlated Setting	
	3.5 Auto Save		
	3.6 Color Settin	Ig	
	3.6.1 Modify		
	3.6.2 Modify		
	3.7 The Flow of		
4	4.12 Multi of	to Logic Analysis	
	4.12 Wulli-St	sic	
		unalveis	
	4 3 Plug Analys	ie	
	Plug Introduction	מר	
	4 4 Rus Packet	l ist	
	4 5 Rus Analysi	e	120
	4.5.1 Genera	al Rus Analysis	
	4.5.2 IIC Ana	alveis	
	4.5.2 107 m	ftware Basic Setup of Protocol Analyzer IIC	
	4522 Pro	ntocol Analyzer IIC Timing Analysis	128
	4523 Pro	ntocol Analyzer IIC Packet Analysis	129
	4.5.3 UART	Analysis	
	4.5.3.1 Sof	ftware Basic Setup of Protocol Analyzer UART	
	4.5.3.2 Pro	otocol Analyzer UART Packet Analysis	
	4.5.4 SPI An	alvsis	
	4.5.4.1 Sot	ftware Basic Setup of Protocol Analyzer SPI	
	4.5.4.2 Pro	otocol Analyzer SPI Packet Analysis	
	4.5.5 1-WIRE	E Analysis	
	4.5.5.1 Sot	ftware Basic Setup of Protocol Analyzer 1-WIRE	
	4.5.5.2 Pro	otocol Analyzer 1-WIRE Packet Analysis	
	4.5.6 HDQ A	nalysis	
	4.5.6.1 Sot	ftware Basic Setup of Protocol Analyzer HDQ	153
	4.5.6.2 Pro	otocol Analyzer HDQ Packet Analysis	159
	4.5.7 CAN 2.	0B Analysis	160
	4.5.7.1 Sot	ftware Basic Setup of Protocol Analyzer CAN 2.0B	160
	4.5.7.2 Pro	otocol Analyzer CAN 2.0B Packet Analysis	169
	4.6 Compressio	on	170
	4.6.1 Softwa	re Basic Setup of Compression	

	4.7 Signal Filter and Filter Delay	
	4.7.1 Basic Setup of Signal Filter and Filter Delay	
	4.8 Noise Filter	
	4.8.1 Basic Software Setup of Noise Filter	177
	4.9 Data Contrast	
	4.9.1 Basic Software Setup of Data Contrast	
	4.10Refresh Protocol Analyzer	
	4.10.1 Basic Software Setup of Refresh Protocol Analyzer	
	4.11Memory Analyzer	184
	4.11.1 Basic Software Setup of Memory Analyzer	
	4.12Multi-stacked Logic Analyzer Settings	
	4.12.1 Basic Software Setup of Multi-stacked Logic Analyzer Settings	
5	Troubleshooting	190
	5.1 Installation Troubleshooting	191
	5.2 Software Troubleshooting	
	5.3 Hardware Troubleshooting	
6	FAQ	194
	6.1 Hardware	
	6.2 Software	
	6.3 Registration	201
	6.4 Technical Information	
	6.5 Others	
7	Appendix	205
	7.1 Hot Keys	





This Quick Start Guide is designed to help new and intermediate users navigate and perform common tasks with the Zeroplus Logic Analyzer. Despite its simple packaging and interface, the Logic Analyzer is a sophisticated measurement and analysis tool. It is also a highly sensitive electrical current sensing device. Users must carefully read instructions and procedures pertaining to installation and operation. Any instrument connected to the unit should be properly grounded. A pair of anti-static gloves is strongly recommended when performing a task with the device. To ensure accuracy and consistency of output data, use of the bundled components is strongly recommended.

Users' opinions are very important to Zeroplus. Please contact our engineering team by telephone, fax or email with your questions or feedback. Thank you for choosing the Zeroplus Logic Analyzer.



# 1 Features of Zeroplus Logic Analyzer

- 1.1 Package Contents
- 1.2 Introduction
- 1.3 Hardware Specifications
- 1.4 System Requirements
- 1.5 Device Maintenance and Safety



# Objective

In this chapter, users will learn about the package contents, description, hardware specifications, system requirements, and safety issues of the Zeroplus Logic Analyzer. Although this chapter is purely informative, we highly recommend reading this carefully to ensure safety and accuracy when performing any operation with the Zeroplus Logic Analyzer.

# 1.1 Package Contents

Verify the package contents before discarding packing materials. The following components should be included in your product. For assistance, please contact our nearest distributor.

Models	LAP-C (16032)	LAP-C (16064)	LAP-C (16128)	LAP-C (32128)	LAP-C (321000)	LAP-C (322000)
Logic Analyzer	1	1	1	1	1	1
16-Pin Testing Cable	0	0	0	1	1	1
8-Pin Testing Cable	2	2	2	2	2	2
Probe	2	20	20	36	36	36
USB Cable	1	1	1	1	1	1
Quick Start Guide	0	1	1	1	1	1
Driver CD**	1	1	1	1	1	1
1-PinTesti ng Cable (White)	1	1	1	1	1	1
2-Pin Testing Cable (Black)	1	1	1	1	1	1

Table	1-1:	Parts	List	for	Retail	Packages	
I UNIO		1 41 60	-101			i uonugoo	

\* This Driver CD consists of a multilingual software interface program, as well as a multilingual User Manual.



孕龍科技股份有限公司 Zeroplus Technology Co., Ltd.

Fig. 1-7: 1-Pin External Clock Cable (White)



Fig. 1-2: Testing Cable



Fig. 1-4: USB Cable



Fig. 1-6: Driver CD

Fig. 1-8: 2-Pin Ground Cable (Black)



## 1.2 Introduction

Zeroplus Logic Analyzer LAP-C Series share the same external features as illustrated in the following figures.



Fig. 1-9: A View of the Zeroplus Logic Analyzer LAP-C Series. See *Fig 1-11* for detailed information on the **Signal Connectors** 



Fig. 1-10: Side View of the Zeroplus Logic Analyzer; the power of the Logic Analyzer is drawn from the USB connection.



Fig. 1-11: Side View of the Zeroplus Logic Analyzer LAP-C Series



Models	LAP-C (16032)	LAP-C (16064)	LAP-C (16128)	LAP-C (32128)	LAP-C (321000)	LAP-C (322000)
Port A ( <b>A0~A7</b> )		$\checkmark$		$\checkmark$	-	V
Port B ( <b>B0~B7</b> )		$\checkmark$		$\checkmark$	$\checkmark$	
Port C ( <b>C0~C7</b> )		Х		$\checkmark$	1	V
Port D ( <b>D0~D7</b> )	Х			$\checkmark$		
R_O	$\checkmark$				1	$\checkmark$
T_0	$\checkmark$			$\checkmark$	-	$\checkmark$
S_0	$\checkmark$			$\checkmark$	1	$\checkmark$
CLK	$\checkmark$			$\checkmark$	1	V
GND	$\checkmark$			$\checkmark$	1	$\checkmark$
VDD	$\checkmark$			$\checkmark$	1	V
IOA	$\checkmark$			$\checkmark$	٦	V
IOB	$\checkmark$				1	$\checkmark$
IOC					1	$\checkmark$
GND	$\checkmark$				r	$\checkmark$

#### Table 1-2: List of Functional Pins in Each Model

#### Table 1-3: Definitions and Functions of Pins for All Models

CLK	Clock	Connect a given external module to be analyzed.		
GND	Ground	Two pins used for grounding the Logic Analyzer with a given external module to be analyzed.		

#### Table 1-4: Definitions and Functions of Pins for Advanced Models (1)

R_0	Read (Out)	When the Logic Analyzer is about to upload data from the memory to the PC, the <b>R_O</b> will send a <b>Rising</b> <b>Edge</b> signal of DC3.3V. When the upload is finished, a <b>Falling Edge</b> signal is sent.
T_0	Trigger (Out)	When a trigger condition is established, the <b>T_O</b> will send a <b>Rising Edge</b> signal of DC3.3V. When the memory is full, a <b>Falling Edge</b> signal is sent.
\$_0	Start (Out)	When a user initiates a sampling task by clicking the RUN icon in the window or clicking the START button on the device, the <b>R_O</b> will send a <b>Rising Edge</b> signal of DC3.3V. When the Logic Analyzer finishes uploading, a <b>Falling Edge</b> signal is sent.

#### Table 1-5: Definitions and Functions of Pins for Advanced Models (2)

VDD	Voltage Drain	Provide +3.3 V for external modules by draining	
VDD	(Semiconductor)	voltage from the Logic Analyzer.	
10.4	Ext. I/O Modulo A	Transmit signals between an external model or	
IUA	Ext. I/O Module A	device and the Logic Analyzer.	
IOB	Ext. I/O Module B	Same as <b>IOA</b> .	
IOC	Ext. I/O Module C	Same as IOA.	
GND	Ground	Ground external devices in sequence.	



# 1.3 Hardware Specifications

ltems\Models	LAP-C (16032)	LAP-C (16064)	LAP-C (16128)	LAP-C (32128)	LAP-C (321000)	LAP-C (322000)	
Interface			USB	2.0 (1.1)		1	
Operating System			WinME/2	000/XP/VIST	٩		
Power Supply		US	SB 1.1 (USB	2.0 Recommended)			
Channels		16			32		
Bandwidth		75MHz		7	75MHz		
Memory	512K Bits	1M Bits	4M Bits	4M Bits	32M Bits	64M Bits	
Memory Depth (Per Channel)	32K Bits	64K Bits	128K Bits	128K Bits	1M Bits	2M Bits	
Internal Clock Rate (asynchronous)	100 ~ 1	00MHz	100 ~ 200 MHz	0 100 ~ 200 MHz			
Max External Clock (synchronous)	Max 75MHz		Max 100MHz	Max 100MHz			
Trigger Channel		16 Channel	s	32 Channels			
Trigger Condition			Edg	je/Pattern			
Pre-Trigger/ Post-Trigger				Yes			
Trigger Level			1	1 Level			
Trigger Count	1-65535						
Max Trigger Page	Max 8192						
Filter Channel		16		32			
Bus Data Decoding	Yes						
Filter Delay			Start: Edg End	ge and Pattern I: 1-65535			
Compression	Со	16 Channel, Compression 1-255			24 Channel, Compression 1-255		



## **1.4** System Requirements

This section discusses basic operating system and hardware requirements for the Logic Analyzer. Software and hardware capabilities may vary depending on PC configuration. This manual assumes proper installation of a supported operating system as listed below.

### 1.4.1 Operating System Requirements

In this sub-section, we share our experiences in testing the Zeroplus Logic Analyzer on the following Microsoft Windows operating systems. Since the Zeroplus Logic Analyzer requires the operating system support of the USB protocol, Windows 95r2 and earlier OS versions are incompatible.

- 1) Windows NT 4.0 (Workstation & Server, Service Pack 6) not supported
- 2) Windows 98, 98 Second Edition not supported
- 3) Windows ME supported
- 4) Windows 2000 (Professional, Server Family) supported
- 5) Windows XP (Home, Professional Editions (32-Bit versions)) supported
- 6) Windows Server 2003 Standard Edition, Enterprise Edition, Small Business Edition (32-Bit Versions) not supported
- 7) Windows Vista (32-Bit and 64-Bit version) supported



### 1.4.2 Hardware System Requirements

• CPU

WinME 166MHz, or above Windows 2000, XP 300 MHz, or above (strongly suggest 900 MHz, or above). Windows Vista 800MHz, or above

We have tested various 32-Bit and 64-Bit CPUs. Overall, we find that all 32-Bit CPUs work very well with Logic Analyzer software. Moreover, we find that AMD's 64-Bit CPUs, except Opteron, with a 64-Bit Windows operating system, work just fine with Logic Analyzer; no significant problems occur.

#### • Memory

WinME 128 MB or above Windows 2000, XP 256 MB or above (128 MB minimum). Windows Vista 512 MB or above

- Hard Drive
   At least 100 MB available space.
- USB USB 1.1 compatible (recommend USB 2.0).
- **Display Devices** (recommended) VGA Display Capability with 1024x786 resolution or higher.



# **1.5 Device Maintenance and Safety**

Follow these instructions for proper operation and storage of the Logic Analyzer.

#### Table 1-7: General Advice

Cautions	<ul> <li>Do not place heavy objects on the Zeroplus Logic Analyzer.</li> <li>Avoid hard impacts and rough handling.</li> <li>Protect the Logic Analyzer from static discharge.</li> <li>Do not disassemble the Zeroplus Logic Analyzer; this will void the warranty and could affect its operation.</li> </ul>
Cleaning	<ul> <li>Use a soft, damp cloth with a mild detergent to clean.</li> <li>Do not spray any liquid on the Zeroplus Logic Analyzer or immerse it in any liquid.</li> <li>Do not use harsh chemicals or cleaners containing substances such as benzene, toluene, xylene or acetone.</li> </ul>

Table 1-8:	Electrical	Specifications
------------	------------	----------------

Items	Minimum	Typical	Maximum
Working Voltage	DC 4.5 V	DC 5.0 V	DC 5.5 V
Current at Rest			200 mA
Current at Work			400 mA
Power at Rest			1 W
Power at Work			2W
Error in Phase Off*			± 1.5 nS
V <sub>input</sub> of Testing Channel			± DC 30 V
V <sub>Reference</sub>	DC -6		DC +6 V
Input Resistance		500KΩ/10pF	
Working Temperature	5°C		70°C
Storage Temperature	-40°C		80°C

\* Refer to the User Manual for error analysis calculation.



孕龍科技股份有限公司 Zeroplus Technology Co., Ltd.

#### Table 1-9: Operating Environment

WARNING	<ul> <li>Avoid direct sunlight         <ul> <li>Use in a dust free, non-conductive environment (see Note)</li> <li>Relative Humidity: &lt; 80%</li> <li>Altitude: &lt; 2000m</li> <li>Temperature: 0 ~ 40 Degrees C</li> </ul> </li> <li>This is a Class A product which may cause radio interference in a domestic environment.</li> <li>Note: EN 61010-1:2001 specify degrees of pollution and their requirements. Logic Analyzer falls under Level 2.</li> <li>Pollution refers to 'addition of foreign matter, solid, liquid or gaseous (ionized gases), which may produce a reduction of dielectric strength or surface resistivity'.</li> <li>Pollution Degree 1: No pollution or only dry, non-conductive pollution occurs. This pollution has no effect.</li> <li>Pollution Degree 2: Normally only non-conductive pollution occurs. Occasionally, however, temporary conductivity caused by the condensation must be expected.</li> <li>Pollution Degree 3: Conductive pollution occurs or dry, non-conductive pollution which becomes conductive due to the condensation occurs. In such conditions, the equipment is normally protected against exposure to direct sunlight, precipitation and wind, but neither temperature nor humidity is controlled.</li> </ul>
Storage Environment	Relative Humidity: < 80% Temperature: 0 ~ 50 Degrees C

# Conclusion

After reading this section, users should have a basic grasp of the Logic Analyzer. A complete understanding of the section, **Device Maintenance and Safety**, is a critical prerequisite of any further operation as presented in the User Manual.



# **2** Installation

- 2.1 Software Installation
- 2.2 Hardware Installation
- 2.3 Tips and Advice



## Objective

This chapter describes the installation of the Logic Analyzer hardware and software. Software installation steps must be followed precisely to ensure successful installation.

## 2.1 Software Installation

In this section, users will learn how to install the software interface and drivers. As with proper installation of many USB devices, the Logic Analyzer application and driver software must be installed prior to the connection of the hardware. The following steps illustrate an installation of a Zeroplus LAP-C(16128) Logic Analyzer. The other five models mentioned in Chapter 1 would follow identical procedures.

- Step 1. Insert the driver CD-ROM in the PC CD drive.
- **Step 2.** Execute the installation program. Go to the START menu, click **START**, **Run**, **Browse in sequence**, select **Setup.exe** file in the appropriate model folder and then click **OK**. It is recommended that all other programs are closed while the installation proceeds.
- Step 3. Choose the desired language.
- Step 4. Click Next to proceed with the Install Wizard.
- Step 5. Select "I accept the term in this license agreement ", and click Next.
- Step 6. Enter User and Organization name.
- Step 7. Choose the setup type. We recommend Complete for most users.
- Step 8. Click Install to confirm settings and begin the actual installation.
- Step 9. Click Finish to complete the installation.
- Step 10. Click Yes to restart the PC.







# 2.2 Hardware Installation

孕龍科技股份有限公司

Technology Co., Ltd.

Hardware installation simply involves in connecting the Logic Analyzer to your computer with the included USB Cable as shown in Figures 2-4 and 2-5.





At this point, the computer should be able to detect the Logic Analyzer and finalize the installation for hardware connection. For further information, refer to the Troubleshooting and Frequently Asked Questions (FAQ) chapters in the User Manual.



Fig. 2-6: An Assembly of Laptop, Logic Analyzer, and a Testing Board



# 2.3 Tips and Advice

- 1. When testing a circuit board, make sure that the internal sampling frequency (within the Logic Analyzer) is at least four times higher than the external board frequency.
- 2. If the signal connector does not work well with the pins on the test board, try to use the supplied probes.



- 4. The Logic Analyzer will connect to the **Zeroplus** server for software updates if an internet connection is available.
- 5. Unwanted signals can be filtered out using the **Signal Filter** or **Filter Delay** functions.
- 6. When measuring for a long period, **Compression** makes memory more efficient.
- 7. Trigger condition depends on the testing board. If triggering does not work well, try to narrow the trigger conditions and optimize them repeatedly.
- 8. If a testing board has a lower frequency than Logic Analyzer, sample signals according to the external clock.
- 9. When sampling from an external clock, filter extra signals with the Signal Filter function.
- 10. Unused channels may be removed from the Bus/Signal display using Bus/Signal (Menu) → Channels Setup.



# **3 User Interface**

- 3.1 Menu & Tool Bars
- 3.2 Find Data Value
- 3.3 Statistics Feature
- 3.4 Customize Interface
- 3.5 Auto Save
- 3.6 Color Setting
- 3.7 The Flow of Software Operation



## Objective

Chapter 3 presents detailed information on the Logic Analyzer software interface in four sections: **Menu Bar**, **Tool Bar**, **Statistical Function**, and **Interface Customization**.

# **Basic Layout**

The layout of the Logic Analyzer software interface can be divided into nine sections as shown in the following figure.



Fig 3-1: Software Interface

#### 1. Menu Bar

All operations are performed directly from the menu bar, including **configure label**, **rename**, **execute** and **stop**. Pull-down menus allow easy navigation through the measurement panel.

#### 2. Tool Bar

The tool bar is the graphical user interface which can make you work with some of the more common applications. From these icons, you can change settings and operate the Logic Analyzer easily.

#### 3. Information Bar

The Information Bar displays information about the grids in the waveform. For example: Address, Time, Frequency, Trigger Bar, A Bar, B Bar and other Bar. Details of the labels are below:

Scale - Define the acquisition clock that controls the data sampling

Total - The period of time when Logic Analyzer captures data.

Display Pos - The middle tip means the middle position of the waveform.

Trigger Pos - Trigger position.

A Pos - The main function is to set A Bar or the other Bar.

B Pos - The main function is to set B Bar or the other Bar.

A-B - Press the under arrow to exchange and become the other Bar Moreover, you also can execute this function from the other Bar.

#### 4. Ruler (Waveform Display / Listing Display)

Ruler shows the time position of the waveform shown in the waveform display area or the listing display area.

#### 5. Bus/Signal (Waveform Display / Listing Display)

Edit names of the measured channels; color shown matches the trace color.

#### 6. Trigger Column



Trigger Column allows users to adjust signal trigger conditions.

#### 7. Filter Column

Filter Column allows users to set Bus or signal filter conditions.

#### 8. Display Area

Acquired data is displayed as a waveform or in a list format.

#### Waveform Display

This interface shows the digital signals. When the signal is logic "0", the waveform will be displayed as \_\_\_\_\_\_. If the signal is logic "1", the waveform is as \_\_\_\_\_\_. An unknown signal waveform is displayed in gray between the high and low levels as \_\_\_\_\_\_. There are sixteen channels in LAP-C(16032), LAP-C(16064) and LAP-C(16128), and thirty two channels in LAP-C(32128), LAP-C(321000) and LAP-C(322000).

#### **Listing Display**

This interface shows the digital signals as 1 and 0. Logic 1 is displayed as "1" and logic 0 is displayed as "0".

#### 9. Status Area

Display Logic Analyzer status. The function name is also indicated here.



#### 3.1 Menu & Tool Bars

Section 3.1 presents detailed information on the eight menu and thirteen tool items shown in the menu bar. The eight menu items are File, Bus/Signal, Trigger, Run/Stop, Data, Tools, Window and Help. The thirteen tool items are Standard, Trigger, Run/Stop, Sampling, Trigger Content Set, Display Mode, Windows, Mouse Pattern, Zoom, Data, Show Time/Height, Trigger Delay and Font Size.

### 1. File

	New Open	Ctrl+N Ctrl+O	← Close - Close the file being worked on.
	Close	Ctrl+F4	
H	Save	Ctrl+S	←Auto Save - Save the required file
	Save As		automatically (See Section 3.5 for detailed
2	Auto Save		instructions)
6	Export Waveform	Ctrl+Shift+E	← Export Waveform - Export files into Text
æ	Export Packet List		(*.txt) and CSV Files (*.csv)
io:	Capture Window	Ctrl+C	← Export Packet List – Export the active
	Language	•	packet list.
5	Print	Ctrl+P	language interface of menus, tool boxes,
	Print Preview		etc
	Print Setup		<b>Frint Preview</b> - Show three options:
2	<u>1</u> IIC. als		Bus/Signal & Trigger & Filter, Position
	Exit		Display Area and Waveform Display (See
			<b>Exit</b> Exit the program

Fig 3-2: File menu.

- e active
- ange the boxes,
- options: Position lay (See
- Exit Exit the program. ÷



Fig 3-3: Standard Tool Bar.



### Menu Bar: File

Menu li	tem	Detail Menu & Dialog Box	
New New	Ctrl+N	Open a <b>New</b> file.	
		Прев	<u> 7 ×</u>
		Lack, ix 📋 My Decuments 💿 🗮 🛍 😁 📼 -	
Dpen	Ctrl+0	Hi Remonia Hy Reserve Disk Mop My Desuments My Desuments Hy Desuments	
		Figure	Upen
		Files of types Logic Analyzer LAPIC File(", alc)	Daned
		- Mile Provides	
		Project: Date: Author: Time:	
		Title: Module No:	
			1
			14

Fig 3-4: Open an existing file.



		Save As					<u>?</u> ×
		Sever	🔁 Ns Documen	6	•	- 🗈 🖆 🖾-	
		Ny Record December 10 December 10 Desiration Hy December 10 Hy December 10	My Music My Music My Hutanus				
E Save	Ctrl+S	Mp Tons.ter					
		Nis hierowak Places					
Save As							
			Filegane			•	Save
💾 Auto Save			Serelas ypec	Logie And Joen LAP C File (*	le]	*	Cancel
		File Note Projecti L Ticibi a Note:	efrojest nos karann	Auton SUSANFA	<b>1</b> 5		2
							5

Fig 3-6: Save As Dialog Box

Save - Save the current file. Save As - Specify the name of the file to be saved.

Auto Save - Save the required file automatically.



Bus Output Parameter: Decide whether to or not to display the parameters of the file to be exported.

Perform Model: Choose whether to export the data either vertically or horizontally.

Data Style : Include ALL, ALL BUS, SPEC BUS (HAS CHANNELS ), SPEC BUS(NO CHANNELS).

Data Model: Export data changed function; the selected items include ALL data, Sampling changed (Compression), Data changed (Compression). Some of the data value for



the signal channels of sampling position are the same, for example, view the data changed and decrease export capacity; this function will be good for users.

# **Output Range:** Choose the range of the data to export from the pull-down menus.

**pop up an export file automatically**: The export file can be popped up automatically. Users can decide whether to activate the function; the default is selected. See the export file below:

🕞 Export File - Notepad	
Bie Edit Format Yew Help	
Thanks for using ZEROPLUS Logic analyzed	4
//Filename: Export File.txt //File size:182 KB	
<pre>// File created on: 2009/03/26 / cogic Analyzer setup information sampling mode standard innern3 sampling frequency = 200000 Hz / more use Data Compression. The number of charmel = 2 / The setup : The part of the setup is the set</pre>	
// Channel name: A0 A1 A2 A3 A4 A5 A6 A7 B0 B1	
V/Trigger: D D D D D D D D D	
//Sieve out the display of the data. The style of the bata's display of Bus is Hexadecimal. A Bar position: -15 T Bar position: 0 B Bar position: 15	•
4	14



eport Packet Lis	1					1
Save in:	🞯 Desktop		-	🗕 🛍 🔶	*	
My Recent Documents	My Documents My Computer My Network PI LAP-A Standar LAP-8 V3.04.0 LAP-C Standar PlugInsA V3.03.04 User Export File	aces d V3.04.01 2009-03 2_Beta_08 2008-08 d_V3.04.01 2009-0 Manual.EN(080811	-11 -26 3-25 )			
My Computer						
Places	File <u>n</u> ame: Save as <u>t</u> ype:	Text Files(*.txt)		•	·]	jave ancel
Bus Output Para	No He	cter Model	Exp	ort Format	Optic	m.,,
-Output Range -						
Fron	First Packet	<u> </u>	To F	inal Packet	<b>-</b>	
	0		Γ	)		

Fig 3-9: Export Packet List Dialog Box

Users can use paperwork, register and analyze packet list data.

**pop up an export file automatically**: The function of popping up an export file automatically in the Export Packet List dialog box is the same with that of the Export Waveform dialog box.

**Export Format**: The Export Format is convenient for users to ues the captured data in the following process. There are two formats for selecting, Report Form and Pure Data Form. See the following picture:

🧰 Export Packet List...



Bus Output Parameter Character Model	Export Form
Output Range	Pure Data Form
From First Packet	To Final Packet
0	0
v pop up an export file automatically	

Fig 3-10: Export Format Pull-down Menu In the part of the Export Format, when the users select the Report Form, the "Option" button can't be used; when users select the Pure Data Form, the "Option" button can be used. The "Option" pops up the Option dialog box as follows, where users can customize the export data items in the dialog box which are Packet #, Name, TimeStamp, Length and Describe.

Option	×
Options	
☑ Packet#	🔽 Length
🔽 Name	🔽 Describe
🔽 TimeStamp	
	OK Cancel

Fig 3-11: Option Dialog Box

For instance, all the export options are selected entirely. See the below picture:



Fig 3-12: Pure Data Form



📷 Capture Window

	🔐 Capture Window	×
Ctrl+C	Capture to Note: Cilpboard MSPaint Capture Region Capture Region Select Region	
	Selection line color	✓ opposite of color
	Note text color	
	Capture	Cancel

#### Fig 3-13: Capture Window

This feature is equivalent to [Alt]+[Print Screen], or [Print Screen]

#### Capture to

File – Save the captured image as either a jpeg or bmp
 Clipboard – Copy the captured image to the clipboard for use in other applications.

MSPaint – Directly start MSPaint to view the captured image.

#### **Capture Region**

- Full Screen - Capture everything on the screen.

 Select Region – After pressing the capture button, a cross-hair will appear on the screen. Left click the mouse button to drag an area to capture.

**Selection Line Color** – Click the color box to change the color.

**Opposite of color** – Click this check box to ensure that the note text will be the opposite of the line color.

Note text color- Choose the color of the note text.

**Note** – Type in a note to attach to the captured image.

Capture - Click the button to capture the image.

Cancel - Click Cancel to end the capture.

	Chinese(Si) Chinese(Tr) Image: English Fig 3-14: Choose among Chinese Simplified (Si), Chir Traditional (Tr) and English.	iese
Language 🕨 🕨	ZEROPLUS Logic Analyzer	1
	The program needs to restart. Do you want to save the current document?	
	Fig 3-15: When changing languages, the above scre be displayed and the program will need to be restart	- en will ed.



	Seneral	<u>?×</u>
	Select Printer	-
🚑 Print Ctrl+P	Status: Print to file Preferences. Location: Comment: Fing Printer	
	Page Range         © All         © Selection       © Current Page         © Pages:	
		el

Fig 3-16: Click to enter the **Print** dialog box.



Fig 3-17: Click to show a **Preview** of the **Print**.

	Print Setup
	Printer       Microsoft Office Document Image Writer       Properties         Status:       Ready         Type:       Microsoft Office Document Image Writer Driver         Where:       Microsoft Document Imaging Writer Port:         Comment:       Comment
Print Setup	Paper       Orientation         Sige:       Letter         Source:       Default tray         Network       OK
	Fig 3-18: Click to enter the <b>Print Setup</b> dialog box.
Recent File	Show the recently saved file.



## 2. Bus/Signal

₩, 2,	Sampling Set Channels Se	:up . tup						Sa	-Clock Source	lock		
	Group into B Ungroup fro	us m Bu	15	a a	trl+( trl+l	<b>5</b> J			Internal Clo     Frequency:	ck 200KHz		
[	Expand Collapse								Synchronous Clo	ock		
	Format Row Rename					Þ		Aut Mor	to Size ve Left/Up	ck dge dge		
hann	els Setup				A	vdd		Hid Sha	le DW All	ternal cloc	:k '	VC
Tr. FiJ	Port Condition Condition		X	X				Col	or RAM Size: 2k	<b>_</b>		-( ]
A	0 1	7	6 6	5 5	4	3 3	2 2		Channel number limited to 32	will be		

Fig 3-19: **Bus/Signal** Menu. Dialog boxes of the Sampling Setup and Channels Setup are shown and indicated by arrows.



Fig 3-20: Trigger Tool Box.



Tip:

lcon

₩

I∰I

лл

ហារប

Description

Decrease

RAM Size

Increase

RAM Size

Decrease Internal

Clock Frequency Increase Internal

Clock Frequency

Menu Item	Detail Menu & Dialog Box
	Sampling Setup
🎬 Sampling Setup	Clock Source Asynchronous Clock Frequency: 200KHz Synchronous Clock C External Clock C External Clock C Rising Edge Frequency: 100KHz C Falling Edge (Min:0.001Hz, Max:100MHz) Note: The external clock voltage level is the same as the port A trigger level
	Sampling RAM Size RAM Size Channel number will be limited to 32

Fig 3-21: Sampling Setup

See Section 4.1 for detailed instructions.



#### Fig3-22: RAM Size

Choose the RAM size and the internal clock frequency from the pull-down menus.

RAM Size	The amount of the acquired data that can be stored by the Logic Analyzer depends on the amount of the allocated RAM.
	The total depth of the memory for the LAP-C is 128K Bits in each probe.
	If the Logic Analyzer starts gathering data with a 128K memory range, it will take a long time to find the required information.
	In order to avoid spending a lot of time gathering data, select a smaller RAM size. The RAM size options are 2K, 16K, 32K, 64K, 128K and 256K. So, if gathering data with 128K takes a long time why does 256K make sense? The reason for this extra RAM size is to cope with the fact that
	a few of the $1 \sim 16$ channels may have a large data input.

FM07I4A



#### Tip:

Clock Source Asynchronous Clock

/ Synchronous Clock					
Asynchronous Clock					
Internal Clock					
Frequency:	50KHz 💌				
	100Hz				
Synchronous Clock	500Hz 1KHz				
C External Clock	5KHz				
C Dicion Edi	25KHz				
<ul> <li>Naling Edg</li> </ul>	50KHz				
C Falling Ed	100KHz				
Notes The set	200KHz				
Note: The exte	400KHz				
	800KHz				
	1MHz				
Sampling	10MHz				
- DAM Size	25MHz				
RAM 5/28	50MHz				
RAM Size: 24	80MHz				
121	100MHz				
Channel number w	150MHz				
limited to 32	200MHz				

Use the pull-down menu to choose the speed of the clock on the board being tested.

The sampling frequency should be more than 4 times higher than the signal to be measured so that the waveform duty cycle depiction will be accurate.

Synchronous Clock



Compression

Tip:

D

Choose the frequency of the clock on the board of the Logic Analyzer. Select "External Clock" to acquire data through external sampling. Choose either "Rising Edge" or "Falling Edge" to execute the analysis process.

According to the users input the value of external frequency in software, the software can count the relevant value about signal mode and frequency. For example: the value of the message, the time scale and the zoom in and out will be the value of time mode.

#### **Connecting the Synchronous Clock**

Use one of the single connecting cables to put one end on the testing board and the other in the LA as shown in the diagram opposite.

Check the box to compress all the data.

Compression is used to compress acquired data through a lossless compressor. The purpose of this compression is to place more data in a limited memory than in an actual memory. The compression rate of the Logic Analyzer can be up to 255 times. This means that the maximum acquisition can be 32M Bits (128Kx255= 32M Bits) for each channel. The chosen capacity of the memory, 1MB, means that the maximum data being sieved out arrives at 1MB\*255=255M Bits (Per Channel).

**Note:** The rate will change depending on the data being analyzed.



Fig 3-23: Signal Filter Setup Dialog Box

Tip:

Click to enter the signal filter setup dialog box.

The function of Signal Filter is to use an alterable judgment circuit which can filter undesired signals in order to capture and store valuable data in the memory. When the combination of input signals from each channel meets the filter conditions, the section of acquired data will be gathered by the Logic Analyzer and stored in the memory. After storing the data, it will return to the Logic Analyzer's system and be displayed as a waveform. If the combination does not meet the filter conditions, it won't gather and store data.

Tip:

There are three modes of Signal Filter configuration for each channel.

1. **Solution** = Don't Care means that the Logic Analyzer captures all signals from sampling.



Fig 3-24: High and Low Levels

It is the system default.

2. High Level means that the Logic Analyzer captures and displays the input signals satisfying the high level.

3. **EXAMPLE** = Low Level means that the Logic Analyzer captures and displays the input signals satisfying the low level.









Fig 3-27: Expand



Fig 3-29: Click to change the Bus or signal display.

TIP:					
Format Row					
Auto Size ( it is not available in Waveform Display mode) Move Left/Up (change to Move	Changes the display of a Bus or a signal. Size the signal columns automatically.				
Left in Listing Display)	Highlight a signal or Bus and click <b>Move Left/Up</b> to move the signal or Bus up (left) through the list of the				
Move Right/Down (change to	Bus/signal.				
Move Right in Listing Display)	Highlight a signal or Bus and click <b>Move Right/Down</b> to move the signal or Bus down (right) through the list of the				
Hide	Bus/signal.				
Show All	Highlight a signal or Bus and click <b>Hide</b> to hide it.				
Color	Click to show all signals and Buses that have been hidden.				
	Highlight a signal or Bus and click <b>Color</b> to change the color.				
Rename	Highlight a signal or Bus and click <b>Rename</b> to rename the Bus or signal.				

**T**:---


# 3. Trigger



Fig 3-30: Trigger Menu



Fig 3-31: Trigger Tool Box



🐢 Bus Trigger

### Menu Bar: Trigger

Menu Item

Detail Menu & Dialog Box

	Bus Trigger Bus Trigger Protocol Analyzer Trigger	×
Setup	Bus Name Operator Value Bus1  = Data Format C Binary C Decimal  ASCII	
	OK Cancel Default Help	

Fig 3-32: Set Bus Trigger

See Section 4.1 for detailed instructions.

	Channel	l Trigger Setup								X
			7	6	5	4	3	2	1	0
	Renta	Filter Condition	$\boxtimes$	$\boxtimes$	$\boxtimes$	$\boxtimes$	$\boxtimes$	$\boxtimes$	$\times$	$\times$
	TOTEX	Trigger Condition								X
	PortB	Filter Condition	$\boxtimes$	$\boxtimes$	$\boxtimes$	$\boxtimes$	$\boxtimes$	$\boxtimes$	$\boxtimes$	$\boxtimes$
rigger Setup	TOTO	Trigger Condition	X							
	RentC	Filter Condition	$\boxtimes$	$\boxtimes$	$\boxtimes$	$\boxtimes$	$\boxtimes$	$\boxtimes$	$\bowtie$	$\boxtimes$
	TOPIC	Trigger Condition	X							
	RentD	Filter Condition	$\times$	$\mathbf{X}$	$\mathbf{X}$	$\mathbf{X}$	$\times$	$\otimes$	$\times$	$\times$
	rortb	Trigger Condition	$\square$							
			ОК		Cancel	R	estore De	faults	Hel	p

Fig 3-33: The trigger action tells the Logic Analyzer when to send data to the PC. The trigger conditions determine when the trigger point starts to record the information.

j <sub>⊤</sub> Trigger Mark	Open the Trigger Mark function.
	See Section 4.1 for detailed instructions.
🔀 Don't Care	Set the trigger condition as " <b>Don't Care</b> " See Section 4.1 for detailed instructions.
Hi gh	Set the trigger condition as " <b>High</b> " See Section 4.1 for detailed instructions.
Low	Set the trigger condition as " <b>Low</b> " See Section 4.1 for detailed instructions.
🗶 Rising Edge	Set the trigger condition as " <b>Rising Edge</b> " See Section 4.1 for detailed instructions.
Falling Edge	Set the trigger condition as " <b>Falling Edge</b> " See Section 4.1 for detailed instructions.
🗙 Either Edge	Set the trigger condition as " <b>Either Edge</b> " See Section 4.1 for detailed instructions.

📲 Trigger Property ..

Trigger Content Setup

Decrease

position

Description

trigger position

Increase trigger

Trigger Page

Trigger Count

Reset
-------

Tip:

lcon

\*

4

N/A

N/A

Reset the trigger condition.

	Trigger Content Trigger Delay	Trigger Range	
-	Trigger Level       Port A       TTL     1.5       Y)       Port B       TTL     1.5       Y)       Port C       TTL     1.5       TTL     1.5       Y)       Port D       TTL     1.5	Trigger Count 1 (Min:1, Max:85535)	

#### Fig 3-34: Set Trigger Content

See Section 4.1 for detailed instructions.

#### **Trigger Level**

The voltage level that a trigger source signal must reach before the trigger circuit initiates a sweep. There are 4 ports available; each port has the ability to assign different voltages to meet the users' requirements. Use the pull-down menu to choose between TTL (default TTL), CMOS (5V), CMOS (3.3V), ECL and User Defined (choose the value of the Trigger Level – 6.0V to 6.0 V).



Fig 3-35: Trigger Position, Trigger Page, Trigger Count

(1) Represents the Trigger Position of a memory page.

- (2) Represents the Trigger Page.
- (3) Represents the Trigger Count.

Tip:			Trigger Property
	Tr	igger Delay	Trigger Content Irigger DeLay Trigger Range
-	lcon	Description	Trigger Page     C Delay Time and Clock     Trigger Page     Trigger Delay Time
-	N/A	Trigger Delay	1         20us           (Min:1, Max:8192)         (Min:20us , Max:335.524s)
			Trigger Position     Trigger Delay Clock       50%     0Min:1, Max: 16776191)
			T Pos = 0 , Start Pos = -1023 , End Pos = 1025 Note: When more than one trigger pages are selected, the trigger bar disappears from the view.
			OK Cancel Default Help
			Fig 3-36: Set Trigger Delay
			See Section 4.1 for detailed instructions.
			Trigger Delay 5us
			Fig 3-37: Set up Trigger Delay clock under time mode.



Trigger Delay 1000

Fig 3-38: Set up **Trigger Delay** clock under sampling site mode.

The **Trigger Delay** setting in **Tool Box** equals to that in the above dialog box.

Tip:			Trigger Property
	Tri	gger Range	Trigger Content   Trigger Delay Trigger Range
-	lcon	Description	Range Setting
_	N/A	Trigger Range	Time Sample V I minute V
			OK Cancel Default Help
			Fig 3-39: Set Trigger Range



4. Run/Stop



Fig 3-40: Run/Stop Menu



Fig 3-41: Run/Stop Tool Box

#### Menu Bar: Run/Stop Menu Item Detail Menu & Dialog Box Click to run once. Single Run F5⊳ See Section 4.1 for detailed instructions. Click to run continuously until the Stop button is ▶▶ Repetitive Run F6 pressed. See Section 4.1 for detailed instructions. Click to stop the repetitive run. 🚺 Stop F7 See Section 4.1 for detailed instructions.



# 5. Data

<b>⊭</b> ₩ <b>▼</b>	Select an Analytic Range Noise Filter Data Contrast		
翻 戸 (+ +)	Find Data Value Find Pulse Width To the Previous Edge To the Next Edge	<b>Ctrl+F</b> F11 F12	
+ ¥ Bar ■¥ Bar	Go To Add Bar Delete Bar	► Alt+A Alt+B	Tak Go To TBar T Bak Go To A Bar A Bak Go To B Bar B Bak Go To B Bar B
2000 2000 2000 2000	Zoom Hand Normal	E H ESCAPE	Go To More
· 2 🛍 🦌 🥦	Zoom In Zoom Out Show all Data Previous Zoom	F9 F8 F10 Ctrl+Z	Binary Decimal ✓ Hexadecimal ASCII
	Data Format Waveform Mode List Data Mode	> > >	C Reverse Square waveform Sawtooth waveform
			All Data Sampling Changed Dot(Compression) Data Changed Dot(Compression)

Fig 3-42: Data Menu

	🖹 👻 🖑 🎬 💹 🕶 👗	100% 🔹		A¥ B¥ Bar Bar	Te +	10	l <b></b>	\$[
--	---------------	--------	--	------------------	------	----	-----------	-----

Fig 3-43: Data Tool Box



# Menu Bar: Data

Menu Item	Detail Menu & Dialog Box				
🔀 Select an Analytic Range	Check the box to enable the Analytic Range to be changed by dragging the Ds and Dp bars with the left mouse button.				
	<b>Noise Filter</b> : It can filter 0~10 Clock's positive pulse width or negative pulse width signal.				
Moise Filter	Noise Filter				
	Fig3-44: Noise Filter See Section 4.8 for detailed instructions.				
	Data Contrast Settings     ▼       ✓ Activate Data Contrast				

	Contrast File LaDoc1 Contrast File LaDoc2 Contrast Beginning Point © T Bar © Beginning of Data	
	Contrast Result           A0[A0]         PASS           A1[A1]         PASS           A2[A2]         PASS           A3[A3]         PASS           A4[A4]         PASS           A5[A5]         PASS           A6[A6]         PASS           A6[A6]         PASS           B0[B0]         PASS           B1[B1]         PASS	Error Stat.
Jata Contrast	Roll the contrast waveforms synchronization     Display files the contrast differences     Display files horizontal     OK Clo	Pin Assignment Perform Contrast Ise Help

### Fig3-45: Data Contrast

Data Contrast: It is used to contrast the difference for the two files of the same style. One is the Basic File, and the other is the Contrast File. The contrast file can display the difference between the Basic File and the Contrast File.



👪 Find Data Value ..

Waveform-Find	8			×
🗌 Activate the	function of Chain-D	ata-Find		
Bus/Signal Name				
Bus1		▼ Next F	Previous Close	
Bus Item:	Find:	Min Value:	Max Value:	
Data	-		FFFFFFF	
Start At:	End At:	When Found:	_ Statistic	1
Ds	▼ Dp	<b>T</b>	Statistic	
103				

Fig 3-46: Waveform-Find Dialog Box without

Activating the Function of Chain-Data-Find Use the pull-down menu to select the Bus/ Signal Name:

The list of Find depends on whether it is a Bus or Signal that is being searched in:

**Bus** – Choose among =, !=, In Range and Not In

Range (enter the value for Min Value and Max Value).

**Signal** – Choose among Rising Edge, Falling Edge, Either Edge, High and Low.

**Start At** - Choose the position to start our search by selecting one of the following:

Ds, T, A, B, ect. (select from the pull-down menu).

When Found - Choose A, B or other bars to mark the

position where it is coincident with the set conditions.

**Statistic** – Show the number of instances of the search results.

Note: It is available only when searching through a Bus.

Waveform-Find	×
Activate the function of Chain-Data-Find	
Bus/Signal Name:	_
Bus1   Next Previous Close	
Please key in a chain of data with a comma to compart them, for example, 32, 45, 50,	66.
01,02,03	
Start At: End At: When Found: Statistic	
Ds The Statistic	

Fig3-47: Waveform-Find Dialog Box with Activating the Function of Chain-Data-Find

Tip:

The function of Chain-Data-Find is mainly for finding the data in the packets of Bus and Protocol Analyzer which have some serial data. For example, it can start finding with the serial packet segments (there are 0X01, 0X02 and 0X03) in the Bus. it



#### improves the efficiency of Data Find. See the

### following process:

Waveform-Find	4
Activate the function of Chain-Data-Find	
Bus/Signal Name:	
Bus1 Next Previous Close	
Bus Item: Find: Min Value: Max Value:	
Data 🔽 = 🔽 0 FFFFFFF	
Start At: End At: When Found: Statistic	
De Tatistic	
Ţ	
Waveform-Find	1
Bus/Signal Name:	
Bus1 Next Previous Close	
Please key in a chain of data with a comma to compart them, for example, 32, 45, 50, 66.	
Start At: When Found: Statistic	
Ds V Dp V A V Statistic	
Û	
Waveform-Find	1
Activate the function of Chain-Data-Find	
Bus/Signal Name:	
Bus1 Next Previous Close	
Please key in a chain of data with a comma to compart them, for example, 32, 45, 50, 66.	
01,02,03	
Start At: End At: When Found:	
Ds V Dp V A V Statistic	

Fig 3-48: Process of Activating the Function of

Chain-Data-Find

142 2948		Bright Trigge	de Wi de S	10	1.307 + 1.151 +		1-1-1	÷	
8115.04	Trigge	-Tilter		WEAR, 99,7		1.1974		ALC: NO.	HEAT
Bull			OXLE	OX1P	01100	03001	00002	0103	OI
	-	-	1			-	1	-	1
	Strate Station Ration Ration	en the Lore d Lance will in chart i	na d'Carlois E F Stariet - con		heise .	2007   2.4.75.16			-
	- Mark Str.		bella .	Hite Facilit	10400				_
100									

Fig3-49: Function of Chain-Data-Find Displayed on

the Waveform Window



💻 Find Pulse Width..

Pulse Tidth-Fi	nd		×
Signal Name: A1	-	Next Previous	Close
Find: In Range 💌	Min Pulse Width:	Max Pulse Width:	Statistic
Start At:	End At:	When Found:	1028

Fig3-50: Pulse Width-Find Dialog Box

Tip:

This function is mainly used for finding the pulse width in a single channel and the single channel of a Bus. It improves the efficiency of finding the Pulse Width for engineers and strengthens the Find function of the Logic Analyzer. **Signal Name:** It can select the single channel for Find. **Find:** It can select the Find conditions which are "In Range", "Min Value", ">", "<" and "=". When users select the option of "In Range", they can input the value of the Min Pulse Width and Max Pulse Width between 1 and 65535 and find the Pulse Width in range. When users select the "Min Value", they can find the Min Pulse Width for the present single channel. When users select the options ">", "<" and "=", they can input the value of the Pulse Width between 1 and 65535 and find the Pulse Width in range.

**Start At:** Select the Start point of Find. The selectable items are all Bars; the default is the Ds Bar.

**End At:** Select the End point of Find. The selectable items are all Bars; the default is the Dp Bar.

When Found: Select a Bar to mark the found Pulse Width. The selectable items are all Bars; the default is A Bar.

**Statistic:** It can count the number of Pulse Width in the present range.

**Next:** It can find the next Pulse Width.

Previous: It can find the previous Pulse Width.

For example: Find in the A1 channel; the Pulse Width is equal to "1"; take the A Bar as the mark. See the below figure:



0 📽 🖬 🍯 🛙	16 II. M	1 7 -		2K •	🛍 🚧 100KHz	50%	· · Page
	1 15	1 k ki ()		400%	2 8 8 L	2 A 14 (C)	I Hei
Scale 0.25 Tetal 2048		Display 1 Trigger 1	tvs760 tvs. 0	A Fes702 B Fes. 15	•	A - T = T09 - B - T = 15 -	
Bus/Signal	Trigger	Filter	-114112	11. 111. 1. 111.	15 -767 J	15 -766 5 -765 25	-764
- Post	181 -	8.	oxs)ox9)ox	A OXB OXC	DXD OXE OX	o)0x1)0x2(0x:	)OX4 OX5
100	131	51	1 1 1	1 1	1 2	1 1 1	1 1
- 🖌 AL 11	- 181	false Tidth	-Tind			× 2	2
- 120	25	Signal Name:		Next	Previous Clo	- 1	
- <b>(</b> 1) =	18	Find:	Pulse Width:	_	Statistic		8
- <b>* M</b> 44	8	Start At:	End At:	When Found:	Statis	<u>6</u>	6
<b>1</b> 45 40	10	Di Address: -769	• Dp	• A	•		32
× 45 10	8	8		63			54
- 100	M	181		127		1	28



Window



Fig 3-53: The selected bar will be shifted to the center of the waveform area.



Add Bar...

Alt+A

Add user defined bars.

- 1. Click the above menu item from **Data** menu, or click **Add Bar** icon from **Tool Bar**.
- 2. Give a **Bar Name**, define a **Bar Color**, and set a **Bar Posi**tion.
- 3. Define the **Bar Key** with the number between 0 and 9.

#### Tip:

The number shortcut is set in the Add Bar dialog box. Every new bar can be filled in one number which is used to find the required bar faster; the default number of the new bar is 0. It is noticed that once the number key is set, it can't be modified, and each new bar can named with the same number, that is to say, one number can name many bars.

For example, users can set the number 3 as the shortcut key. When users press the number 3 key, the C Bar will be displayed in the centre position of the screen.

dd Bar		×
– Setting – Bar Name	с	OK Cancel
Bar Color		
Bar Pos	0	
Bar Key	3	





Fig3-55: Add Bar with the number between 0 and 9

<mark>-</mark> ⊉ Delet Ba⊦	e Bar	Alt+B
Delete a u	ser defined ba	ar.
1. Click the menu, or <b>Tool Bar</b>	above menu i click <b>Delete</b>	tem from <b>Data</b> <b>Bar</b> icon from
2. Select a	user defined	bar, and click
on <b>Delete</b>	<b>e</b> .	
3. Delete ti	he selected	Bar with the

3. Delete the selected Bar with the **Delete** key on the **Keyboard.** Use the mouse to select the added bar and press the **Delete** key on the keyboard to delete the bar.



Fig3-56: Delete Bar Dialog Box





Fig 3-57: Delete a selected Bar.







Fig 3-59: To **Zoom Out**, left click and drag the mouse/point from right to left.



#### Tip:

A Zoom-In or a Zoom-Out view will be centered in the Waveform Display Area, and the new zoomed view will be sized according to the available space on the display.



When users activate the **Zoom** to zoom in / zoom out the selected area, the Tooltip on the right corner of the bottom will display the Time, Clock or Address of the selected area. When selecting the Zoom function, and users are pressing and dragging the left key, the information on the right corner of the bottom will be changed and updated with the width of the selected area. And the information is displayed on the right corner of the bottom in the way of Tooltip. When users loosen the mouse, the information will disappear.

#### **Tooltip:**

Time/Frequency Sample: xxx (time)

/ns (unit)

Address: xxx (There is no unit with the

address.)





Fig 3-60: To display the Tooltip, left click and drag the mouse/point from right to left or from left to right.



# Fig 3-61: Click **Hand**, and then depress and hold the left mouse button to drag.

R Normal ESCAPE	Reset the mouse function to the system default.
nn F9	A Po B Po
K Zoom Out F8	50 , <u>300 ;</u>
Tip: Zoom In and Out can be switche by changing the percentage value i	d n Fig 3-62: Normal Status



the pull-down list.

1. The system can set the value of Zoom In and Out:

The default unit is  $\mu$ s. When zooming in, it will be automatically changed to ns. When zooming out, it will be changed to ms, s or ks.

2. Pull-down Menu:

There are thirty scales. The maximum zoom in and out is the cycle of each grid, 0.0001piece. The minimum zoom in and out is the cycle of each grid, 1,000,000,000.

Zoom in and out (the proportion): with each grid being the cycle, the zoom in and out (%) is 100%. The time of Zoom In and Out counts by the clock of each grid (sample frequency). For example:

(1) Each grid is being a cycle; the zoom in and out is 100%. The time of Zoom In and Out will be presented by the clock of each grid X (1/sample frequency).

(2) Each grid stands for the clock of 100 pieces, the zoom in and out is 1% and the time of Zoom In and Out will be displayed by the cycle of each grid X (1/sample frequency).



Fig 3-63: Result from Normal to Zoom In



Fig 3-64: Result from **Normal** to **Zoom Out** 



Fig 3-65: Show all Data







Fig 3-69: Reverse

The Zeroplus Logic Analyzer User's Manual V3.05

Tip:

This function of Reverse is to reverse the collected signal. Change the High Level into the Low Level; change the Low Level into the High Level. The Reverse of Waveform Mode displays with the dashed, so it is easy to distinguish.



Fig3-70: Reverse Dialog Box

Select All: Select all the signals to start the function of

Reverse.

Clear All: There is no signal to be reversed when

clicking this button.

OK: Start the function of Reverse.





Fig3-71: Reverse Function Displayed in the Waveform Window

#### List Data Mode

#### Tip:

The data for list mode are so many, to be convenient for users, that there is adding a List Data Mode function. The formats for the List Data Mode are All Data, Sampling Changed Dot (Compression) and Data Changed Dot (Compression).

×

All Data: It is the present display mode.

#### **Sampling Changed Dot**

(Compression): Take the sampling changed dot as the compression data reference dot.

Data Changed Dot (Compression):

Take the present data change dot as the compression data reference dot.







# 6. Tools



Fig 3-73: Tools Menu



Fig 3-74: Show Time/Height Tool Box



#### Menu Bar: Tools Menu Item

🧮 Customize

Detail Me	nu & Dialog Box
Customize	
Common Setup Toolbars Sh	ortcut Key Auto Save
Waveform Display Mode Sampling Site Display Time Display Frequency Display	
Ruler Mode C Regular Ruler C Time/ Sampling Site Bulk	Waveform Setting Waveform Height 40 -
Correlated Setting	
Auto-Close	Open/Close Compression Warning
Show Gridline	Open/Close Double Warning
Data Process What do you want to show running? © Keep the Present Data	when you press the Stop during the
Check for Update	

Fig 3-75: Customize Dialog box

See Section 3.4 for detailed instructions.

Eustomize	×
Customize Common Setup Toolbars Shortcut Key Auto Save Toolbars Standard Trigger Run/Stop Sampling Trigger Content Set Display Mode Windows Mouse Pattern Zoom Data ShowTime/Height Trigger Delay	×
OK Cancel Help	
Fig 3-76: Toolbars Setting	



Customize		×
Common Setup   Toolbars   S	hortcut Key Auto Save	
Commands:	Current Keys:	
Add Bar Capture Window	Alt+A	Assign
Close Delete Bar Down End		Remove
Esc Export Waveform F2 F3	1	Reset All
Currently affected to :	Select New Shortcut Key:	
Description: + 🖌 Add Bar Ba+		
	OK Cancel	Help

Fig 3-77: Shortcut Key Setting

Customize X
Common Setup   Toolbars   Shortcut Key   Auto Save
Activate         File Name:         Save Path Name:         D:\My Documents\LA Data         Repetitive Run         Time Interval:         ① Every Renewal         ① Only Display the First File
OK Cancel Help

Fig 3-78: Auto Save Setting

See Section 3.5 for detailed instructions.



T:000000	-0000) - [La	Doc3:1]					
Run/Stop	Data Tools 1	indow <u>H</u> elp		1	_	The second	
φ <sup>2</sup> <del>Υ</del> Τ <del>Υ</del>	u 🛄 🔚 Cust	omize Time of Wavefor	(m.		• m	r ⊀ <b>⇔ 50%</b> -	
R R 🖉	<mark>*≚</mark> ∰60 14 →J 🔞						
Display Pc						A - T = 15	
	- 🛶 Refr	esh Protocol An	alyzer			-	
Filter	🔔 🚃 Memo	ry Analyzer			23 -:	136.957 -130	
	] 1. 📑 Mult	i−stacked Logic og Waveform	Analyzer Setti	ngs	1		
	2222	2222	2222	22	22	2222	
	4 4	4 4	4 4	4	4	4 4	
	8	8	8	8		8	
	16	1	6		16		
	32		32				
			64				

😿 Show Time of Waveform











BUS Bus Property.

C. Consul Dur	Calax Canfin
<ul> <li>General Bus</li> </ul>	
Activate the Latch Function	n A0 🗾
	Rising Analysis
Protocol Analyzer Setting	
C Protocol Analyzer	Parameters Copfig
ZEROPLUS LA IIC MODULE V     ZEROPLUS LA SM 2.0 MODU     ZEROPLUS LA SM 2.0 MODU     ZEROPLUS LA PM 1.1 MODU	/1.08 LE V1.02 LE V1.04
© ZEROPLUS LA IIC MODULE V © ZEROPLUS LA SM 2.0 MODU © ZEROPLUS LA 9-WIRE MODU © ZEROPLUS LA 3-WIRE MODU © ZEROPLUS LA HOQ MODULE © ZEROPLUS LA HOQ MODULE © ZEROPLUS LA I2C(EEPROM 3	/1.08 LE V1.02 LE V1.02 JLE V1.01 V2.05 24LX) MODULE V1.03

Fig 3-82: Bus Property

**General Bus**: Activate the function of analyzing the General Bus.

**Color Configuration**: Open the Color Configuration dialog box to set the conditions for the General Bus.

Activate the Latch Function: Activate the latch function.

**Protocol Analyzer:** Activate the function of analyzing the Protocol Analyzer.

**Use the DsDp**: Use the Ds and Dp to help analyze the Protocol Analyzer.

**Find:** Find the desired Protocol Analyzer module. Users can input the Protocol Analyzer name to quickly find the Protocol Analyzer module from many Protocol Analyzers. After inputting the first character of the name in the Find box of Bus Property dialog box, the corresponding module will be displayed in the Protocol Analyzer list box according to the input character. See the figure below:

Bus Property	X				
- General Bus Setting					
C General Bus	Color Config				
Activate the Latch Function	A0 💌				
	Rising Analysis				
Protocol Analyzer Setting					
Protocol Analyzer	Parameters Config				
C ZEROPLUS LA IIC MODULE V1.08 C ZEROPLUS LA SM 2.0 MODULE V1.02 C ZEROPLUS LA PM 1.1 MODULE V1.04 C ZEROPLUS LA 3-WIRE MODULE V1.01 C ZEROPLUS LA HOQ MODULE V2.05 C ZEROPLUS LA I2C(EEPROM 24LX) MODULE V1.03					
Use the DsDp Find					
More Protocol Analyzer: http://www OK	zeroplus.com.tw Cancel Help				

Fig 3-83: Find Editor Box

See Section 4.5 for detailed

instructions.



When you input "I" in the Find editor box, the Protocol Analyzer list displays all Protocol Analyzers with the initial character of "I"; see the below picture:

Bus Property	×
General Bus Setting	
C General Bus	Color Config
🗖 Activate the Latch Function	A0
	Rising Analysis
Protocol Analyzer Setting	
Protocol Analyzer	Parameters Config
C ZEROPLUS LA IIC MODULE VI.08	3 ) MODULE V1.03
✓ Use the DsDp	Find I
More Protocol Analyzer: http://www OK	w.zeroplus.com.tw Cancel Help

Fig 3-84: Find Result

 Refresh Protocol Analyzer interface.

 Be Section 4.10 for detailed instructions.

	Multi-stacked Logic Analyzer Settings
	Activate Stack
	Stack Type
	Memory Stack
	C Channel Stack
	Please select the Logic Analyzer for stacking
	M1 S/N:000000-0000
	M2 S/N:000000-0000
	M3 S/N:000000-0000
stacked Logic Analyzer Settings	M4 S/N:000000-0000
	- Synchronous Channel
	Synchronous Trigger Condition
	Rising Edge
	OK Cancel Help

Fig 3-86: Multi-stacked Logic Analyzer Settings Dialog Box See Section 4.12 for detailed instructions.

👭 Analog Waveform

📑 Multi-

#### Tip:

When the function of Analog Waveform is activated, the Analog Waveform will be displayed in the waveform area of the General Bus's sub-channel and take the space of four channels. And four subchannels won't draw the waveform. It notes that the sub-channel of the General Bus must be more than four channels.



Fig 3-87: Analog Waveform Diagram

The function of Analog Waveform means that the Display Mode of Bus Data is not the Pure Data Mode, while it displays data change with the curve which looks like a waveform, which, in fact, is a curve to describe the data change. So it is called the Analog Waveform.



7. Window

<ul> <li>Waveform Display</li> <li>Listing Display</li> <li>Hot News Window</li> </ul>	•
Cascade Horizontal Vertical	
✓ <u>1</u> LaDoc1	

Fig 3-88: Window Menu



Fig 3-89: Window Tool Box



#### Menu Bar: Windows Menu Item Detail Menu & Dialog Box 🎼 File Bus/Signal Trigger Run/Stop Data Icols Window Help w 50K Trigger Delay 20us Cascade Display Pos:Ons Scale:20us Total:40.96ms Horizontal Trigger Pos:Ons Vertical Bus/Signal Trigger Filter Waveform Display ✓ 1 LaDoc: 22 $\boxtimes$ $\boxtimes$ 🥖 🗛 🔥 🥖 A1 - A1 $\boxtimes$ $\boxtimes$ $\mathbf{X}$ $\mathbb{X}$ 🥖 A2 A2 $\boxtimes$ $\boxtimes$ $\boxtimes$ 🖌 A4 A4 🥖 AS AS $\boxtimes$ $\boxtimes$

Fig 3-90: Display Signals in Waveform.



Fig 3-91: Display Signals in Listing.

Hot News Window

۰.

#### Tip:

To let online users learn the latest news, we add the

Running-Text Ads Function.

**Turn On**: Start the Running-Text Ads function.

News Activity: Let users learn

the activities of our company.

Production News: Let users







learn the latest products of our company.

Note: If both News Activity and Production News are turned on. The Running-Text Ads will play News Activity prior to Production News, and play the news in order; the whole process plays repetitively.



Fig 3-93: Display Hot News Window on the Software

Interface.

Fig 3-94: Running-Text Ads Interface

#### Packet List

#### Tip:

Setting: Set up the packet list. Refresh: Click it, the content in the packet list will be refreshed. Export: Users can use the fragment to work, record and analyze the packet list data. As Export, according to the packet list arrangement, it exports the text file and csv file.

Synch Parameter: Open the Synch Parameter Setting dialog box.



Fig3-95: Display Packet List





	CLEDING LDG CQ	211.07 (0)	00000 0000)	ELEVES				
	File Bus/Signal Tri	gger Bun/St	op Data Icol	s Mindew Help				
	D 🕼 🖬 🎒 🗯	2. 🖗 🖓	🕶 📲 🍱	<b>&gt; &gt;&gt;</b>	2K 💌 🛗 🔊	100KHz 💌 🚥	4 50%	▼ → Page 1
	🟠 🕓 🗃 🕅	🖬 🥵 🖡	8 👋 🖬 ]	. 100%	- K A	1 12 13 13 M	14 01 5	. · · Heigh
	Trigger Delay	1						
	🐔 Lalloc5			<u>=   0  ×  </u>	🐔 LaBec3			_ [ ] ×
·	1e:1 Display For al:2048 Trigger For	::OA Pos:-15 ::OJ Pos:15	• A - T = 15 • B - T = 15	A - B = 30 - ComportRate:No	1e:1 Display Pe al:2048 Trigger Pe	a:04 Pos:-15 - A a:03 Pos:15 - B	- T = 15 +A - T = 15 +C	- B = 30 - ompr-Rate:No
Horizontal	Dus/Signal	Trigger	Filter 771	50 5 10 12 12 13 10	Dus/Signal	Trigger File	er spp.1-s	• 5 1 0 12 12 13 13 -
	- 🖌 🚾 XO				- 🖌 🚾 AO		1	
	- 🖌 🖬 🕹				- 🖌 AL AL		0	
	- 122			-	- 12 12		1	-
	4 >	• • •		<u>)</u> //	x >	<b>. .</b>	<b>)</b> (	1
	A LaBact			- IDI XI	LaBer?			L D X
	lati Display Par	O PastelS	w A = T = 15   v	A = 3 = 30 ×	leil Display P.	arth PastelS w A	- T = 15   vA	- B = 20 ×
	al 2048 Trigger Pos	08 Pos: 15	B - T = 15	Compr-Rate No	al:2048 Trigger Fo	15:03 Pag:15 - B	- T = 15 +C	onpr-Rate No
				N N N				
	Bun/Signal	Trigger	Filter - Fi	-56 510 2020	Bun/Signal	Trigger Filt	er -55-1-5	8 5 La 20210
	— 🖌 <mark>мо</mark> ло	⊠ •			- 🖌 🚾 10		1	
	— 🥖 🖬 🔺				— 🖌 AL AL		1	
	- / 12 12				- / 12 12		1	
		• • •		1 1/1				1
	Ready						Eadl	DEMO //

Fig 3-97: Align Workspace(s) Horizontally

ITTERAT PARA	1						
LaBocs 14:1 Display I al:2048 Trigger I	fox:OA Fox:=1 fox:OS Fox:15	5 💌 A = T 💌 B = T	= 15 *A - B = 30 * = 15 *Compr-Rate:Ho	LaBort la:1 Display F al:2048 Trigger F	oz:04 Poz:=1 es:03 Poz:15	5 <b>-</b> A - 1 <b>-</b> B - 1	r = 15 +A - B = 3 r = 15 +Conpr-Rate
Bus/Signal	Tricer	Filter	-FF1-585102000-	Bux/Signal	Trigger	Filter	FF-1-57 510-20
ст 🖌 🐱 но				а <mark>а</mark> 🖌 🚽			,
— 🖌 🗛 🔒				- 🖌 🗚 🔺			
- <b>/ K2</b> K2				- / K2 K2			
64 <b>64 5</b>				CA 🖬 🗧			
— 🖌 🗛 🗛				- 🖌 🗛 🗚			
— 🖌 AS AS				— 🖌 🖍 AS			
- 18 15				KB 16			
100	N	100		A 17 17	12	152	1

Fig 3-98: Align Workspace(s) Vertically

#### Stopwatch Function:



Vertical

Fig3-99: Stopwatch Function

The function will show at right corner of the bottom of the screen while sampling data. It times from users pressing the ensured key at the Bus Property dialog box to Bus insert sending back analyzed data. Please look at the left figure.

It has five functions as following:

Time of waiting for triggering, Time of triggering success, Time of sampling data, Time transmitted to computer after sampling data finished and Time of Bus data overloading.



# 8. Help

	Logic Analyzer Help	F1
	Keyboard Map	
	Report a Problem	
?	About ZEROPLUS Logic Analyzer	
	About ZEROPLUS More Protocol Analyzer	

Fig 3-100: Help Menu



### Menu Bar: Help

Menu Item

Logic Analyzer Help

Detail Menu & Dialog Box



Fig 3-101: Open Logic Analyzer Help file.

	👔 Hot Key ¥iew		
	Orders	Hot kev	
	Place the A Bar position	۵.	Move waveform to where takes A-
	Place the B Bar position	 B	Move waveform to where takes R-
	Place the T Bar position	т	Position T-Bar to the center of dis
	Change to Enclose mode	E	Change the mouse mode to Enclo
	Change to Hand mode	- н	Change the mouse mode to Hand
	Put A Bar	Ctr1 + A	Put A-Bar on the center of display
•	Put B Bar	Ctrl+B	Put B-Bar on the center of displa
	File -> Granh	Ctrl + C	Open the dialogue of Capture Gra
	Data ->Enclose	Ctrl + E	To transfer the mode of mouse is
	Data -> Find Data Value	Ctrl + E	Search specific data with predet
	Bus/Signal -> Group into Bus	Ctrl + G	Group selected signals into Bus
	File -> New	Ctrl + N	Create a new file
	File -> Onen	Ctr1 + 0	Onen saved file
em -	Report a problem to the s	ervice e-m	nail at:
	Report a problem to the s service_2	ervice e-m @zeroplu:	nail at: s.com.tw
	Report a problem to the s service_2	ervice e-m @zeroplu: 	nail at: s.com.tw
	Report a problem to the s service_2	Cervice e-m @zeroplus LAP-C Series Version : Sta	nail at: s.com.tw ndard V3.04.01(090306)
	Report a problem to the s service_2	Cervice e-m Ceroplus LAP-C Series Version : Sta S/N:000000-	nail at: s.com.tw ndard V3.04.01(090306) 0000
	Report a problem to the s service_2 About ZEROFLUS Logic Analyze ② 孕龍科技設份有限公 Zeropla Technology Co., Li The Information of the Version New Feature:	Cervice e-m Ceroplus LAP-C Series Version : Sta s/N:000000-	nail at: s.com.tw ndard V3.04.01(090306) 0000
	Report a problem to the s service_2 About ZEROPLUS Logic Analyze ② 孕龍科技設份有限公 Zeropla Technology Co., Li The Information of the Version New Feature: Find Pulse Width Analyze Hundhaw	Caroplus Caroplus LAP-C Series Version : Sta S/N:000000-	nail at: s.com.tw ndard 43.04.01(090306) 0000
<u> </u>	Report a problem to the s service_2 About ZEROPLUS Logic Analyze ② 孕龍科技設份有限公 Zeroptia Technology Co., Li The Information of the Version New Feature: Find Pulse Width Analog Waveform Software Information Display for	22EROPLUS LAP	nail at: s.com.tw ndard \93.04.01(090306) 0000
<u> </u>	Report a problem to the s service_2	Construction of the service of the s	nail at: s.com.tw ndard \3.04.01(090306) 0000
	Report a problem to the s service_2 About ZEBOPLUS Logic Analyze のので見たいのでは、 ア部科技設份有限公式 Zeroptus Technology Coto The Information of the Version New Feature: Find Publes Width Analog Waveform Software Information Display for Software Information Display for Software Information Display for Chain-Data-Find Reverse for waveform	2EROPLUS LAP	nail at: s.com.tw ndard 1/3.04.01(090306) 0000
- Analyzer	Report a problem to the s service_2 About ZEROPLUS Logic Analyze PERMADBAG AGA PERMADBAG AGA PERMADBAG AGA PERMADBAG AGA PERMADBAG PERM	2EROPLUS LAP	nail at: s.com.tw ndard V3.04.01(090306) 0000
ic Analyzer	Report a problem to the s service_2 About ZEROFLUS Logic Analyze PERMADBORGENESS PERMAD	2EROPLUS LAP	nail at: s.com.tw ndard V3.04.01(090306) 0000
 .ogic Analyzer	Report a problem to the s service_2 About ZEROFLUS Logic Analyze PERMADBORGEN PERM	2EROPLUS LAP	nail at: s.com.tw ndard V3.04.01(090306) 0000
em -	Report a problem to the s service_2 About ZEROFLUS Logic Analyze PERMABENGAGENCE. PERMABENGAGENCE. The Information of the Version New Feature: Find Pulse Width Analog Waveform Software Information Display for Chain-Data-Find Reverse for waveform Memory Analyzer Multi-stacked Logic Analyzer Sett Bug Fixed: Detailed description invites reference	2EROPLUS LAP	nail at: s.com.tw ndard V3.04.01(090306) 0000
- Analyzer	Report a problem to the s service_2	Carecopius  Carecopius Carecopius  Carecopius  Carecopius  Carecopius  Carecopius  Carecopius  Carecopius  Carecopius  Carecopius  Carecopius  Carecopius  Careco	nail at: s.com.tw ndard V3.04.01(090306) 0000
ic Analyzer	Report a problem to the s service_2	zeroPLUS LAP	nail at: s.com.tw ndard \93.04.01(090306) 0000
n -	Report a problem to the s service_2 About 2EBOPLUS Logic Analyze Pathology Co.Li The Information of the Version New Feature: Find Pulse Width Analog Waveform Software Information Display for Chain-Data-Find Reverse for waveform Multi-stacked Logic Analyzer Sett Bug Fixed: Detailed description invites reference ( Copyright(C) 1997-2009 ZEROPLUS TH Website: http://www.zeroplus.com.th	service e-m Control Control C	nail at: s.com.tw ndard \(3.04.01(090306)) 0000
 : Analyzer	Report a problem to the s service_2	2EROPLUS LAP	nail at: s.com.tw ndard \(3.04.01(090306)) 0000
- Logic Analyzer	Report a problem to the s service_2	CEROPLUS LAP  CEROPLUS LAP  CEROPLUS LAP  ings  ence "ReadMe"  company website cr4NoLOGY CO., LTT  poout ZERC	nail at: s.com.tw ndard \(3.04.01(090306)) 0000 0. DPLUS Logic Analy

modules.

Tip:

The function of Software Version Information Display for the ZEROPLUS LAP means that the software will open a small window which displays the software version, new functions and bug modifications when activating the software. It is convenient for users to know the information of the present software version.



Fig3-104: Software Version Information Display Window



## Right Key

Menu Item

Detail Menu & Dialog Box

Right Key Menu on the Bus/Signal	
Column	

## Tip:

The Right Key bar is added on the basis of the Bus/Signal Bar. So the function of Sampling Setup, Channel Setup, Group into Bus, Ungroup from Bus, Format Row and Rename are the same as those in the Menu Bar.

EUS	Sampling Setup Channels Setup Bus Property Analog Waveform	
	Group into Bus Ungroup from Bus	Ctrl+G Ctrl+V
	Add Channel Copy Channel Delete Channel Delete All Channels Restore Default Channels	
	Format Row Rename	•

Fig 3-105: Right Key Menu on the Bus/Signal

Column

General Bus Setting	
General Bus	Color Config
Activate the Latch Function	A0
	Rising Analysis
Protocol Analyzer Setting	
C Protocol Analyzer	Parameters Config
O ZEROPLUS LA ISM 2.0 MODULE VI.     O ZEROPLUS LA SM 2.0 MODULE V     O ZEROPLUS LA SM 2.0 MODULE V     O ZEROPLUS LA 3-WIRE MODULE V     O ZEROPLUS LA HOQ MODULE V2.     O ZEROPLUS LA I2C(EEPROM 24L)	V 11.02 11.04 V1.01 05 X) MODULE V1.03
Use the DsDp	Find
More Protocol Analyzer: http://ww	w.zeroplus.com.tw
ОК	Cancel Help

Add Channel	×
Channel: A0	▼ Cancel
Fig 3 107: Add the require	



\_

\_\_\_\_

Bus/Signal column.

Copy Channel	ZEROPLUS Logic Analyzer         Do you want to copy the channel ?         OK       Cancel         Fig 3-108: Copy the selected channel in Bus/Signal column.
Delete Channel	ZEROPLUS Logic Analyzer         Do you want to delete the channel ?         OK       Cancel         OK       Cancel         Fig3-108: Delete the selected channel in Bus/Signal column.
Delete All Channels	ZEROPLUS Logic Analyzer         All the Buses and channels will be deleted. Do you want to continue?         OK         Cancel         Fig 3-109: Delete all Buses and channels in Bus/Signal column.
Restore Default Channels	ZEROPLUS Logic Analyzer       X         All the Buses and channels will restore to the default. Do you want to continue?         OK       Cancel         Fig3-110: Restore the deleted Buses and channels in Bus/Signal Column.

# Right Key Menu on the Waveform Area

#### Tip:

The functions of the right key menu on the waveform area is similar to those of the Data menu.

The menu adds the functions, such as remembering the last setting conditions in the Waveform-Find dialog box, Place Ds and Dp, Add Bar in the waveform area, and so on.



Fig3-111: Right Key Menu on the Waveform Area

Waveform-Fin	d		×
C Activate the	e function of Chain-	Data-Find	
Bus/Signal Nam	e:		
Bus1		Next Previous	Close
Bus Item:	Find:	Min Value: Max Valu	Je:
Data	<b>_</b>  =		
Start At:	End At:	When Found:	
Ds	▼ Dp		atistic
		0	

Fig3-112: Waveform-Find Dialog Box



x Activate the function of Chain-Data-Find Bus/Signal Name • Next Previous Close Bus Item: Data Min Value Find: Max Value: • -• 0 Start At: End At: When Found: Statistic Ds 💌 Dp • A •

Fig3-113: The Result of Finding the Former Set

Conditions

# 🙀 Find Data Value ... Ctrl+F

#### Tip:

Remember the final conditions: When the find function is used, the function of displaying the final conditions is added. When you have closed the Waveform-Find dialog box, and you want to find the set conditions, you can open the Waveform-Find dialog box again for the system has saved the last set conditions. See the figure in the right column.
Place A Bar Place B Bar Place Dp Bar Place More.

### Tip:

The right key menu on the waveform area adds the function of Place Ds and Place Dp. However the functions are only used after the Ds and Dp bars are activated, otherwise they will be disable. These functions are the same as that of A Bar.

When the mouse is stopped at a special position, click the right key on the mouse, select the Place Ds or Place Dp, the Ds or Dp bar will move to the special position.

For example, Open "Select an Analytic Range", select the special position is "-10", and then select "Place Ds". See the figure in the right column.





Fig3-114: Place Ds Bar

### 🕂 Add Bar

### Tip:

When the mouse is located at a special position on the waveform area, click the right key to select the Add Bar function; a bar will be added automatically in the special position according to the sequence of the word and color. See the C Bar in the position "5" in the right column.







Fig3-115: Add Bar on the Waveform Area.



# 3.2 Find Data Value

Find Data Value is a very useful tool to help the user to find data on the received signals.

- **Step1.** Click the find data value icon; the dialog box of Waveform-Find will appear.
- Step2. Using the pull-down menu, select the Bus/Signal Name.

The Bus/Signals listed on the pull-down menu represent the status of the Bus/Signal column as shown in Fig 3-116.



Fig 3-116

Step3. Choose the character for Find. The list of characters depends on whether it is a Bus, Signal, or the protocol analyzer such as IIC/ UART/ SPI, etc., which is being searched (See Figs 3-117, 3-118, 3-119, 3-120, 3-121, 3-122 3-123, 3-124 and 3-125).

General Bus: Choose among = , != , In Range and Not In Range (Enter the Min Value or Max Value).

**Protocol Analyzer:** Choose the segments bits of the protocol analyzer (Select the protocol analyzer item and enter the value for Min Value or Max Value).

Signal: Choose among Rising Edge, Falling Edge, Either Edge, High or Low.

Taveform-Find		X Taveform-Find		×
C Activate the function of Chain-Data-F	ind	C Activate the fun	ction of Chain-Data-Find	
Bus/Signal Name:		Bus/Signal Name:		
A3 🔽	Next Previous Close	(A3	▼ Next	Previous Close
Bus1	Min Value: Max Value:	Bus Item:	Find: Min Value	: Max Value:
A0 A1	▼ FFFFFFF	Data	💌 Rising Edge 💌	FFFFFFF
	When Found:	Start At:	Rising Edge End Falling Edge hen Found	Statistic
Bus2 B0	A Statistic	Ds 🔻	Either Edge	Statistic
B1 B2	0		Low	0
B3				



Taveform-Find	×	Taveform-Find	×
C Activate the function of Chain-Data-Find		C Activate the function of Chain-Data-Find	
Bus/Signal Name:		Bus/Signal Name:	1
Bust Min Value: Max Value:	1	Bus Item: Find: Min Value: Max Value:	
		Data = 00 FFFFFF	
Bus2 When Found:		Start At: End != Pen Found: Statistic	
		Ds Dp Not In Range	
B2 B3			

Fig 3-118: Waveform-Find Dialog Box of the Logic Bus

Taveforn-Find	×	Taveform-Find	×
C Activate the function of Chain-Data-Find		C Activate the function of Chain-Data-Find	
Buc/Signal Name:		Bus/Signal Name:	
Bust Previous Close		Buct Vext Previous Close	
Bust Min Value: Max Value:		Bus Item: Find: Min Value: Max Value:	
		WRITE = FFFFFFF	
A2 A3 When Found: Statistic		START Statistic Statistic	
Bus2 Statistic		READ Statistic	
B2 B3		A-NACK	

Fig 3-119: Waveform-Find Dialog Box of the Protocol Analyzer IIC



Taveform-Find	×	Taveform-Find	×
C Activate the function of Chain-Data-Find		C Activate the function of Chain-Data-Find	
Bos/Signa Name:		Bas/Signal Narge:	
A2 Next Previous Close		► <u>Next</u> Close	
Bust Min Value: Max Value:		Bus Item: Find: Min Value: Max Value:	
		WRITE Rising Edge  FFFFFFF	
A2		Rising Edge	
A3 When Found:		Start At: End Falling Edge hen Found:	
BO Statistic		Either Edge Statistic	
Bi			
B2			
B3	-		

### Fig 3-120: Waveform-Find Dialog Box of the IIC Signal

Taveform-Find	C Taveform-Find	×
Fave fore - Find       Activate the function of Chain-Data-Find       Daty/Signal Name:       Tx Bus       New3       A0       C0       C0       C0       C1	C Tave for = 7 ind Activate the function of Chain-Data-Find Bur/Signal Name: Tx Bus Bus Item: Find: Min Value: Max Valu	×
TXD(A0) RX Bus RXD(A1) When Found: Statistic A V	START 4A: When Found: DATA ODD PARITY STOP ERROR-0 ERROR-1	

Fig 3-121: Waveform-Find Dialog Box of the Protocol Analyzer UART

Taveforn-Find	Taveform-Find X
C Activate the function of Chain-Data-Find	C Activate the function of Chain-Data-Find
TXD(A0	By <del>s)'Byral Na</del> ne: TXD ( A0)
A0 Min Value: Max Value:	Bus Item: Find: MinPosition: MaxPosition:
The Part of the Pound: Statistic Statistic	Start At: Rising Edge Pen Found: Statistic Statistic



Taveforn-Find	X Taveform-Find	×
C Activate the function of Chain-Data-Find	Activate the function of Chain-Data-Find	
Rus/Signal Name: MOST Next Previous Close	BusySignal Name: Most Next Previous Close	e
AU A1 A2 A3	Bus Item:         Find:         Min Value:         Max Value:           UNKNOW </td <td></td>	
Statistic SC(A0) SS(A1) DATA(A2) MISO	DaTA dAt: When Found: Statistic	<u> </u>
SCK(A0)		

Fig 3-123: Waveform-Find Dialog Box of the Protocol Analyzer SPI

Taveform-Find		X Taveform-Find	×
Activate the function of Chain-Data-	Find	C Activate the function of Chain-Data-Find	
Bus/Signal Name:		Bus/Signal Name:	
SCK(A0)	Next Previous Close	SCK(A0)  Next Previous Close	
A0	Min Value: Max Value:	Bos Item: Find: Min Value: Max Value:	
A1 A2	FFFFFFF	UNKNOW I Rising Edge F FFFFFFF	-
MOSI	When Found:	Start At: End Faling Edge hen Found: Statistic	
SC(A0) SS(A1) DATA(A2)	A Statistic	Ds Dp High	
MISO SCK(A0)	<u>lo</u>		



Taveform-Find	Taveform-Find
C Activate the function of Chain-Data-Find	C Activate the function of Chain-Data-Find
Bus/Signal Name:	Bue/Signal Name:           SPI <ul> <li>Next</li> <li>Previous</li> <li>Close</li> </ul>
Bus Item: Find: Min Value: Max Value:	Bus Item: Eind: Min Value: Max Value:
DATA UNKNOW d At: When Found: Statistic	Start At: Endl= hen Found: Statistic
Ds Dp B Statistic	Ds TIN Range Statistic
Address: 600	Address: 600

Fig 3-125: Waveform-Find Dialog Box of the Bus Item of the SPI Signal



Step4. Choose the position to start the search by selecting one of the following: Start At: Ds T, A, B, C, etc.; End At: Dp, A, B, C, etc.. Then click Next or Previous to search it.

When Found: Choose a Bar to mark the result: A, B, C, etc..

Step5. Click Statistic to show the number of instances of the search results.

Note: It is available only when searching through a Bus.



Fig 3-126: The A bar is placed at the 0X08 of Bus1 where the condition of the Waveform-Find is set. The Statistic of Waveform-Find shows a "64".

Scale:0.125 Total:2048		Display Trigger	Pos:-917 Pos:O	A Pos:-917 B Pos:15 ▼	•	$\begin{array}{l} A \ - \ T \ = \ 917 \ \big  \checkmark \\ B \ - \ T \ = \ 15 \ \big  \checkmark \end{array}$
Bus/Signal	Trigger	Filter	-919.5 -91	8.875 -918.25 -917.6	25 -917 -916.375	-915.75 -915.125 -914.5 -913
Busi	× -		) 0X67	0X68 ( 0X6	9 ( OX6A )	OX6B 0X6C (0:
<b>/ AO</b> AC						
🖌 🗚 A1			Taveform-Fi	ind		×
🥖 A2 A2		$\boxtimes$	Activate th	ne function of Chain-Data	a-Find	
🧭 A3 A3	×		Bus/Signal Nan Bus1	ne:	Next Pre	evious
🧭 🗚 A4			Bus Item:	Find:	Min Value:	Max Value:
🖌 🖌 AS		$\square$	Start At:	End At:	When Found:	Statistic Statistic
🖌 🖌 AB		$\square$	Address: -917	7  Dp		0
<b>/ A</b> 7 A1						
🖌 BO BO						

Fig 3-127: The A bar is placed at the 0X6A of Bus1 where the condition of the Waveform-Find is set.



孕龍科技股份有限公司 Zeroplus Technology Co., Ltd.



Fig 3-129: The B bar is placed at the 0X13 of Data of Protocol Analyzer SPI where the condition of the Waveform-Find is set.



# 3.3 Statistics Feature

Section 3.3 presents detailed information on the **Statistics** feature in the software interface. The **Statistics** feature presents user information pertaining to nine periodicities: **Full Period**, **Positive Period**, **Negative Period**, **Conditional Full Period**, **Conditional Positive Period**, **Conditional Negative Period**, **Start Pos**, **End Pos and Selected Data**.

Click on the Statistics icon iii, and an interface like Fig 3-130 or Fig 3-131 will appear.

STAT. VIET									×
Channel Param	eter Item Para	meter Condition	Parameter Wa	rning Parameter	Refresh [	Statistic Filter			
CHANNEL	Full Period	Positive Per	Negative P	Conditional	Conditional	Conditional	Start Pos	End Pos	Selecter 🔺
A0	1020	1020	1020	0	0	0	Ds	Dp	
A1	514	514	514	0	0	0	Ds	Dp	
A2	257	257	257	0	0	0	Ds	Dp	
A3	128	128	129	0	0	0	Ds	Dp	
A4	64	64	65	0	0	0	Ds	Dp	
A5	32	32	33	0	0	0	Ds	Dp	
A6	16	16	17	0	0	0	Ds	Dp	
A7	8	8	9	0	0	0	Ds	Dp	
BO	0	0	1	0	0	0	Ds	Dp	
B1	0	0	1	0	0	0	Ds	Dp	
B2	0	0	1	0	0	0	Ds	Dp	
B3	0	0	1	0	0	0	Ds	Dp	
B4	0	0	1	0	0	0	Ds	Dp	
B5	0	0	1	0	0	0	Ds	Dp	-1
R6	0	0	1	0	0	0	De	Dn ,	





Fig 3-131: Logic Analyzer with Statistics Enabled

There are four options for adjusting how statistical information may be presented. These four options are **Channel Parameter**, **Item Parameter**, **Condition Parameter**, and **Warning Parameter**.



#### **Channel Parameter**

Channel P	aran	neter	•						×
	7	6	5	4	3	2	1	0	
Port A	◄	◄	◄	◄	◄	◄		◄	
Port B	◄	◄	◄	◄	◄	◄	◄	◄	
Port C	◄	◄	◄	◄	◄	◄	◄	◄	
Port D	◄	◄	$\checkmark$	◄	◄	◄	◄	$\overline{}$	
Port E	Γ	Г	Г	Г	Г	Г	Г	Г	
Port F								Γ	
Port G								Γ	
Port H	Γ								
Port I		Γ	Γ	Γ	Γ	Γ	Γ	Γ	
Port J	Γ								
Port K	Г	Г				Г	Г	Г	
Port L									
Port M	Γ	Γ	Γ	Γ	Γ	Г	Г	Γ	
Port N	Γ					Γ	Γ	Γ	
Port O	Γ								
Port P	Г	Г	Г	Г	Г	Г	Г	Г	
Select	all )	Cle	ar all		OK		Ca	ncel	

Fig 3-132: **Channel Parameter**. Allow the choice of pins in which port will be included in the statistical analysis of a test run.

### **Item Parameter**

tem Parameter	×
Probe	
Full Period	
Positive Period	
🔽 Negative Period	
🔽 Conditional Full Period	
Conditional Positive Period	
🔽 Conditional Negative Period	
🔽 Start Pos	
🔽 End Pos	
🔽 Selected Data	
OK Cancel	

Fig 3-133: **Channel Parameter**. Allow the choice of items which will be considered in the statistical results.

### **Condition Parameter**

Condition Parameter	×
Conditional Full Period	7
20us <= Time <= 20us	
Conditional Positive Period	
10us <= Time <= 10us	
Conditional Negative Period	
10us <= Time <= 10us	
OK Cancel	

Fig 3-134: **Condition Parameter.** Allow the setting of time intervals for Conditional Full Period, Conditional Positive Period and Conditional Negative Period.



孕龍科技股份有限公司 Zeroplus Technology Co., Ltd.

Channel Param	ieter Item Para	ameter Condition	Parameter Wa	rning Parameter	Refresh	Statistic Filter			
CHANNEL	Full Period	Positive Per	Negative P	Conditional	Conditional	Conditional	Start Pos	End Pos	Selecter A
A0	1020	1020	1020	0	0	0	Ds	Dp	
A1	514	514	514	0	0	0	Ds	Dp	
42	257	257	257	0	0	0	Ds	Dp	
43	128	128	129	0	0	0	Ds	Dp	
44	64	64	65	0	0	0	Ds	Dp	
45	32	32	33	0	0	0	Ds	Dp	
46	16	16	17	0	0	0	Ds	Dp	
47	8	8	9	0	0	0	Ds	Dp	
30	0	0	1	0	0	0	Ds	Dp	
31	0	0	1	0	0	0	Ds	Dp	
2	0	0	1	0	0	0	Ds	Dp	
33	0	0	1	0	0	0	Ds	Dp	
34	0	0	1	0	0	0	Ds	Dp	
5	0	0	1	0	0	0	Ds	Dp	
86	0	0	1	0	0	0	De	Do	

Fig 3-135: The Numbers of Data Qualified by Condition Parameter

### Warning Parameter

Iarning Parameter     X       Image: Activate Warning Setting				
Conditions	Min	Max		
• Period	🔽 10us	✓ 100us		
C Frequency	L 10KHz	100KHz		
	0	Cancel		

Fig 3-136: Warning Parameter. Set the conditions which will be marked to call users' attention.

STAT. VIET									×
Channel Parame	eter Item Parar	neter Condition	Parameter Wa	rning Parameter	Refresh	Statistic Filter			
CHANNEL	Full Period	Positive Per	Negative P	Conditional	Conditional	Conditional	Start Pos	End Pos	Selecter 🔺
AO	1020	1020	1020	0	0	0	Ds	Dp	
A1	514	514	514	0	0	0	Ds	Dp	
A2	257	257	257	0	0	0	Ds	Dp	
A3	128	128	129	0	0	0	Ds	Dp	
A4	64	64	65	0	0	0	Ds	Dp	
A5	32	32	33	0	0	0	Ds	Dp	
A6	16	16	17	0	0	0	Ds	Dp	
A7	8	8	9	0	0	0	Ds	Dp	
B0	0	0	1	0	0	0	Ds	Dp	
B1	0	0	1	0	0	0	Ds	Dp	
B2	0	0	1	0	0	0	Ds	Dp	
B3	0	0	1	0	0	0	Ds	Dp	
B4	0	0	1	0	0	0	Ds	Dp	
B5	0	0	1	0	0	0	Ds	Dp	- 1
86	0	0	1	0	0	0	De	Do	
1									

Fig 3-137: The numbers of data qualified by warning conditions are printed in black, otherwise in red.



# 3.4 Customize Interface

Section 3.4 presents detailed instructions pertaining to how to **modify** the **Waveform Display Mode**, how to **modify** the **Ruler Mode**, how to **modify** the **Waveform Height**, how to **modify** the **Correlated Setting** and how to use the **Auto Save** function.

🛸 ZEROPLUS LAP-C	(32128)(5/N	:000000-00	100) - [LaDoo	2]								_ 8 ×
🦕 Eile Bys/Signal	Trigger Run/	Stop Data	Tools Wind	ow Help	2K 👻 🛗 🛛		- mar ista	50% <b>v </b>	Page 1	T Cour	. 1	
				- 5 100%			2 商 14	이 [2010] - 4	<ul> <li>Height</li> </ul>	40 -	Trigger D	ielay 1
Font Size 12	~											
Scale:1 Total:2048		Disp Trigg	lay Pos:0 jer Pos:0		A Pos:-15  ▼ B Pos:15  ▼		A- B-	T=15  ▼ T=15  ▼		A - B = 30 Compr-F	) 🚽 ate:No	
Bus/Signal	Trigger	Filter	3	-20	<mark>A </mark> 15	5 .		5	10	, 15,	, 20,	, , , 25 <sup>-</sup>
🖌 🗚 🗛												
🖌 A1 A1												
🖌 A2 A2												
🧭 🗚 🖓												
🖌 🗚 A4												
🖌 A5 A5												
🖌 🗚 A6												
🖋 A7 A7												
🖌 BO BO												
🖌 B1 B1												
🥑 B2 B2												
🥑 <b>B3</b> B3												
🖌 B4 B4												V
Ready			•							F	di	DEMO

Fig 3-138: The Interface Layout Shown in Default Settings



### 3.4.1 Modify Waveform Display Mode

To modify the display mode, users can use icons on the tool bar/box, or menu. For the menu, go to **Tools** and click **Customize**. See *Fig.3-115*.

ars Shortcut Key Auto Save
lav Waveform Setting Waveform Height 40 ▼ Site Ruler ♥ Open/Close Compression Warning ♥ Open/Close Double Warning
to show when you press the Stop during the nt Data  Read the Captured Data Restore Defaults OK Cancel Help

Fig 3-139: Customize the Display Mode by Using the Tool Bar



**Waveform Display Mode** – There are 3 display modes to determine the method of capturing data from sampling: Sampling Site Display, Time Display, and Frequency Display.



### 3.4.2 Modify Ruler Mode

Use the menu to modify the Ruler Mode.

Go to Tools and click Customize. See Fig. 3-142

ustomize						
Common Setup   Toolbars   Shortcut Key   Auto Save						
Waveform Display Mode Sampling Site Display Time Display Frequency Display						
- Ruler Mode	-Waveform Setting					
C Regular Ruler	Waveform Height 40 💌					
Time/Sampling Site Ruler	🗖 Font Size 🛛 🔽 💌					

Fig 3-142: Ruler Mode

### **Regular Ruler**



Fig 3-143: Scales in Regular Ruler

### **Time/Sampling Site Ruler**



Fig 3-144: Scales in Time/Sampling Site Ruler

**Ruler Mode** – There are two styles of Ruler: (Regular Ruler, Time/Sampling Site Ruler) **Regular Ruler:** 

Presented in increments of 5.

Time/Sampling Site Ruler (default):

Presented in increments of 50us.



### 3.4.3 Modify Waveform Height & Correlated Setting

To modify Waveform Height, click **Tools → Customize**.

### **Waveform Height**

Set the height of waveform (18-100) in chosen items at toolbar that will show the amplitude of the waveform.

Ruler Mode	-Waveform Setting			
C Regular Ruler	Waveform Height 🛛 💽			
Time/ Sampling Site Ruler	Font Size 12 🔽			
Correlated Setting				
🔽 Auto-Close 📃 Open/C	lose Compression Warning			
Show Gridline				
Show Tooltip 📃 Open/C	lose Double Warning			
Data Process				
What do you want to show when you press the Stop during the running?				
C Keep the Present Data 💿 Rea	ad the Captured Data			

Fig 3-145: Waveform Height

### Waveform Height = 18

Waveform Height = 40





### **Correlated Setting**

Select Auto-Close in the following figure.

-Ruler Mode O Regular Ruler O Time/Sampling Site Ruler		Waveform Setting       Waveform Height       40       Font Size			
<ul> <li>Correlated Setting</li> <li>✓ Auto-Close</li> <li>✓ Show Gridline</li> <li>✓ Show Tooltip</li> </ul>	C Open/C	Close Compression Warning			
Data Process What do you want to show when you press the Stop during the running? © Keep the Present Data © Read the Captured Data					

Bus/Signal	Trigger	Filter		A) - 986.309	-985.369
Bus1	$\boxtimes$		) 0X03	0 <mark>X</mark> 04 ( 0	)X05
🖌 🖊 AC	$\boxtimes$	$\square$			
🖌 🖌 A1		× -			
🖌 🖊 A2 A2					
🧹 A3 A3					
🥖 🛃 Αζ					
Bus/Signal	Trigge	r Filter	-987.2	<mark>A]</mark> 25 - 986.30	9 , ;985.
Bus/Signal	Trigge	r Filter	0X03	5	9, <u>;985.</u> ) 0X0
Bus/Signal	AC X	r Filter	0×03	∱,	9, <u>.</u> .985. 0X0
Bus/Signal	AC X	r Filter	↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓	986.30 0X04	9, , <u>-985.</u> X 0×0
Bus/Signal	Trigge           A(1)           A(2)	r Filter	↓	6, -986.30 0×04	9, , <u>.</u> 985. (0×0
Bus/Signal Bus1 Bus1 A0 A1 A1 A2 A2 A3	Trigge           At           At           At           At           At	r Filter	• • • • • • • • • • • • • • • • • • •	0×04	9, , ;98 <u>5</u> <u>∕</u> 0×0
Bus/Signal  Bus1 Bus1 A0 A0 A1 A1 A2 A2 A3 A3 A4	Trigge	r Filer	• • • • • • • • • • • • • • • • • • •	<sup>6</sup> , -986.30 0×04	9, , <u>.985</u> 0X0

Fig 3-147: Auto-Close

Fig 3-148: An Example for Auto-Close

Auto-Close - With the cursor in the channel, when users try to drag a Bar, the Bar will stop at the approaching edge of the channel (High Edge or Low Edge).

Tip: In the above example, when dragging the A Bar, the A Bar will stop at the Low Edge of A1.





Fig 3-149: Gridlines

Show Gridline - The gridlines will be displayed on the waveform area.



Fig 3-150 - Tooltips

Show Tooltip – Leave the mouse over a waveform and the description will be shown.

Check for Update: The Logic Analyzer software will automatically check for updates when being started.Restore Defaults: The background color, waveform color, cursor color, text color, grid type and Bus color return to the initial setting.



### 3.5 Auto Save

To save the captured data for a long time, users can use icons on the tool bar/box, or menu.

For the dialog box, go to **File** menu to click **Auto Save** or go to **Tools** menu to select **Customize** and select **Auto Save**. See *Fig 3-151*.

	New	Ctrl+N
È	0pen	Ctrl+0
	Close	Ctrl+F4
	Save	Ctrl+S
	Save As	
•	Auto Save	
<u>6</u>	Export Waveform	Ctrl+Shift+E
œ	Export Packet List	
<b>1</b>	Capture Window	Ctrl+C
	Language	۲.
5	Print	Ctrl+P
	Print Preview	
	Print Setup	
1	IIC. als	
	Exit	

Customize	×
Common Setup   Toolbars   Shortcut Key Auto Save	-1
I✓ Activate File Name: LA	
Save Path Name:	
D:\My Documents\LA Data	
Repetitive Run       Time Interval:       Image: Straight of the	
OK Cancel Help	

Fig 3-151-1: Auto Save on File Menu

Fig 3-151-2: Auto Save Item of Customize

Fig 3-151: Auto Save

Auto Save: The default is not activated; after activating, it keeps working and users also can choose Cancel to close it.

Activate: The default is not activated: after activating, it keeps active and users also can choose **Cancel** to close it. **File Name**: Before users name the file, the file name is defaulted as LA. In fact, the saved file name can add a serial number for the file automatically.

Save Path Name: Users can enter the path directly or choose the path from the selected path button

**Time Interval**: When the auto save function is activated, the time interval from one finished sampling to the next activated sampling can be set according to users' requirements; the default is 1s, and the unit can be selected from s(second), m(minute) and hr(hour).

**Every Renewal**: When the repetitive run is activated, the waveform image or the state image will renew again and again.

**Only Display the First File**: When the repetitive run function is activated, the waveform only displays the first file and it isn't renewed; when the repetitive run is stopped, the waveform still displays the first file.





Fig3-152: Auto Save



# 3.6 Color Setting

To modify Color, click **Tools → Color Setting** 

Name	🔲 Relating	Color	<b></b>
Waveform Background List Background 1 List Background 2 Cursor Grid Unknow Line Default Bus Bus Text List Text Time Text Bus Error Bus Error Text Signal Effer Bar			
	0 0 0 0 0 0 1 1 1	After the bac altered, corre automatically according to ratio .	*kground is esponding color ochange the contrast printed,the is white

Fig 3-153: Workaround and Waveform Color Setting

Workaround – Set the workaround color of the Logic Analyzer and the text.

Name	🔲 Relating	Color	I _
Waveform Background			
List Background 1			
List Background 2			
Cursor			
Grid			
Unknow Line			
Default Bus			
Bus Text			
List Text			
Time Text			
Bus Error			
Bus Error Text			

Fig 3-154: Workaround Color Interface

Waveform Background: The Logic Analyzer's Waveform Viewer Background Color.

- List Background 1: The Logic Analyzer's First Listing Viewer Background Color.
- List Background 2: The Logic Analyzer's Second Listing Viewer Background Color.

All optional items include the current color of Cursors, Grid, Unknow Line, Default Bus, Bus Text, List Text and Time Text (users can scroll the vertical wheel to view the selectable items).

Bus Error: Users can configure the color of Bus Error Data from the Color Setting dialog box.

Bus Error Text: Users can configure the color of Bus Error Text from the Color Setting dialog box.

Relating: When users select one item to change the color of the item, and users want to change other items into

the same color, they can select other items at the same time in the Relating column, then the selected items will be



changed into the same color. So it is convenient for users to change many items into the same color once.

After the background is altered, corresponding color automatically change according to the contrast ratio – When users set the color for the workaround and have selected the option, the system will switch other colors automatically to become the contrast color.

When being printed, the background is white: When being printed, the background color is white.

Waveform - Change the color of the Buses or signals on the waveform area.



Fig 3-155: Waveform Color Interface

Waveform: The channel color can be varied by users.

**Linewidth**: The linewidth can be adjusted by the users' requirements; there are three options which are 1pixel, 2 pixel and 3 pixel.



# 3.6.1 Modify Workaround Color

To modify the workaround color, click the color block shown in Fig 3-154. A **Color** panel, shown in Fig 3-156, will appear. Select a color shown on the panel or click on **Define Custom Colors** to create the desired color.



Fig 3-156: Color Panel with Its Advanced View



### 3.6.2 Modify Waveform Color

Foreground color refers to the color of the output signal lines in the Waveform Display Area. *Fig3-157* presents how to change colors of a signal or some signals. Repeat the following procedures if users need to change colors of many signals.



Fig 3-157: Stepwise Illustration of Changing Waveform Colors

- Step 1: Select several Optional Items.
- Step 2: Select the corresponding items in the relating.
- Step 3: Choose a color by following the method shown in Fig 3-156.
- Step 4: Click **OK** to change their colors into the same, for example A1, A2, A3 and A4.

Here is a sample of an altered Logic Analyzer software interface which will be used for further demonstrations in subsequent chapters. See *Fig 3-158.* 



Fig 3-158: An Altered Interface Sample to Be Used in Subsequent Chapters





# 3.7 The Flow of Software Operation

Fig 3-159: Software Flow Diagram

# Conclusion

Information demonstrated in this chapter is only for entrance level. There are more advanced approaches which may require fewer steps than those shown in this chapter. This chapter is meant to equip users with sufficient grounding of the Logic Analyzer's software interface.



# **4 Introduction to Logic Analysis**

- 4.1 Logic Analysis
- 4.2 Bus Logic Analysis
- 4.3 Plug Analysis
- 4.4 Bus Packet List
- 4.5 Bus Analysis
- 4.6 Compression
- 4.7 Signal Filter and Filter Delay
- 4.8 Noise Filter
- 4.9 Data Contrast
- 4.10 Refresh Protocol Analyzer
- 4.11 Memory Analyzer
- 4.12 Multi-stacked Logic Analyzer Settings



### Objective

Chapter 4 gives detailed instructions on performing two basic analysis operations and five advanced analysis applications with the Logic Analyzer. These two basic analysis operations are the Logic Analysis and the Bus Logic Analysis, which are fundamental to all further applications. The other five advanced analysis applications are the IIC (Inter Integrated Circuit) Analysis and the UART (Universal Asynchronous Receiver Transmitter) Analysis, the SPI (Synchronous Peripheral Interface) Analysis, Compression, Signal Filter Setup, and Filter Delay Setup.

# 4.1 Logic Analysis

Logic Analysis is meant for a single signal analysis. Section 4.1 gives detailed instructions on the software's basic setup.

Basic Software Setup of the Logic Analysis

### Task 1. Clock Source (Frequency) and RAM Size Setup

**Step1.** Click icon or click Sampling Setup from Bus/Signal on the menu bar, the dialog box as shown in Fig 4-1 will appear.

.US LAP-C (32128) (S/1	1:00000-0000) - [LaDoc1]
Bus/Signal Trigger 1	Run/Stop Data Tools Mindow Help
🏬 Sampling Setup	🔤 💽 🕨 🕨 🗔 👬 2K 🔻 👫 🚾 50MHz 👻 🛲
🚜 Channels Setup	Sampling Setup
Group into Bus Ungroup from Bus Expand Collapse	Clock Source Asynchronous Clock  Therenal Clock  Frequency: 50MHz
Format Row Rename	Synchronous Clock  C External Clock  C Rising Edge Frequency: 100KHz  C Falling Edge (Min:0.001Hz, Max:100MHz)  Note: The external clock voltage level is the same as the port A trigger level
	Sampling RAM Size RAM Size: 2k  Compression Mode Compression Mode Signal Filter Signal Filter Setup
	Apply OK Cancel Restore Defaults Help

Fig 4-1 - Clock Source

Step 2. Clock Source (Frequency) Setup

Internal Clock (Asynchronous Clock)

Click on **Internal Clock**, and then select the Frequency from the pull-down menu to set up the frequency of the device under test (DUT). The frequency of the Internal Clock must be at least four times higher than the frequency of the Oscillator on the DUT. Or, select the frequency **200MHz** reference from the pull-down menu on Tool Bar as Fig 4-2 shows.

**Tip:** Connect the output pin of the oscillator from the tested board to the signal connector of the Logic Analyzer to measure it by using the internal clock of the Logic Analyzer.





Fig 4-2 - Clock Source Pull-down Menu

External Clock (Synchronous Clock)

Click on **External Clock**, and then select "Rising Edge" or "Falling Edge" as the trigger condition of the DUT. In the Frequency column, type the frequency of the oscillator on the DUT.

- **Tip:** The External Clock is applied when the frequency of the oscillator on the tested board is exceeds the range of the internal clock of the Logic Analyzer. Connect the output pin of the oscillator on the tested board to the CLK pin of the Logic Analyzer.
- Step 3. RAM Size Setup

Click on the RAM Size **128**K **128**K **f**rom the pull-down menu on the Sampling Setup dialog box as shown in Fig 4-3.



Fig 4-3 - RAM Size

**Tip:** The relationship between RAM Size, Signal Filter Mode, Compression Mode and Channels as shown in Table 4-1 and Fig 4-3.

able 4-1 RAM Size vs Signal Filter Mode	, and RAM Size vs	s Compression Mode	and Channels
---	-------------------	--------------------	--------------

Status		Normal Mo	ode		Double Mo	ode
Model No.	RAM Size/ Channels	Channels Available Compression Mode & Signal Filter Mode		RAM Size/ Channel s	Channels Available	Compression Mode & Signal Filter Mode
LAP-C (16032)	2K ~ 32K	16 channels	Disable	-	-	-
LAP-C (16064)	2K ~ 64K	16 channels	Disable	-	-	-
LAP-C (16128)	2K ~ 128K	16 channels	Available	256K	16 channels	Disable
LAP-C (32128)	2K ~ 128K	32 channels	Available	256K	16 channels	Disable
LAP-C (321000)	2K ~ 1M	32 channels	Available	2M	16 channels	Disable
LAP-C (322000)	2K ~ 2M	32 channels	Available	4M	16 channels	Disable



### Task 2. Trigger Property Setup

Step1. Click icon or click Trigger Property from the Trigger on the Menu Bar. The dialog box will appear as shown in Fig 4-4.

Trigger Run/Stop	Data Tools Y	
♣ Bus Trigger Set ♣ ♥ ♥ ♥ ♥	up • Setup	
Trigger Propert	у	
Trigger Mark	Trigger Property	×
🔀 Don't Care	Trigger Content Trigger Delay Trigger Range	
High Low Rising Edge Falling Edge Either Edge Reset	Trigger Level       Trigger Count         Port A       1.5         TTL       1.5         Y       1.5	
	OK Cancel Default Help	

Fig 4-4 - Trigger Property

Step2. Trigger Level Setup

Click the pull-down menu of **Trigger Level** on Port A, B, C and D to select the Trigger Level as the voltage level that a trigger source signal must reach before the trigger circuit initiates a sweep.

**Tip:** There are four commonly used preset voltages for Trigger Level, TTL, CMOS (5V), CMOS (3.3V), and ECL. Users also can define their own voltage from -6.0V to 6.0V to fit with their DUT. Port A represents the pins from A0 ~ A7 on the signal connector of the Logic Analyzer, and so do Port B, C and D. The voltage of each port can be configured independently.

Trigger Property	×
Trigger Content Trigger Delay Trigger Range	
Trigger Level       Trigger Count         Port A       I         CMOS (5v)       2.5         Port B       (Min:1, Max:65535)         User Defi:       ZEROPLUS Logic Analyzer         Port C       TIL         TIL       Please enter a number between -6.0 and 6.0         Port D       OK	
OK Cancel Default Help	

Fig 4-5 – Trigger Content Error

### Step3. Trigger Count.

Type the numbers or select the number from the pull-down menu of the Count 1 on the Tool Bar or click the pull-down menu of the **Trigger Count** on the Trigger Property dialog box as shown in Fig 4-6.

The system will be triggered at the position where the Trigger Count is set as shown in



Figs 4-6, 4-7 and Fig 4-8.







Fig 4-7 – Trigger Count Screen Shot 1



Fig 4-8 – Trigger Count Screen Shot 2

Step4. Trigger Page/ Delay Time and Clock

The Trigger Page and the Delay Time and Clock can't be applied at the same time.

### 1. Trigger Page:

Click **Trigger Page**, then type the numbers or select the numbers from the pull-down menu of the Page Page 1 • on the Tool Bar or click the pull-down menu of the Trigger Page on the "Trigger Delay" page of the Trigger Property dialog box as shown in Figs 4-9, 4-10 and 4-11. The selected page numbers will be displayed on the screen.

Tip: The Trigger bar (T bar) will not be displayed when the setup of the Trigger Page is more than 1.





Fig 4-11 – Trigger Page and Screen (2)

### 2. Delay Time and Clock

Click the **Delay Time and Clock**, then type the numbers into the column of the Trigger Delay Time or type numbers into the Trigger Delay Clock at the "Trigger Delay" page of the Trigger Property dialog box as shown in Fig 4-11. Or type the numbers into the column of Trigger Delay Trigger Delay on the Tool Bar. The system will display the Start of the waveform.

- **Tip:** The formula of Delay Time and Clock is "Trigger Delay Time = Trigger Delay Clock \* (1/ Frequency)". To use the compression mode, the < Delay Time and Clock > will be unavailable.
- **Step5.** Trigger Position Setup

Type the percentages or select the percentages from the pull-down menu of the 20% and on the Tool Bar or click the pull-down menu of the Trigger Position on the "Trigger Delay" page of the Trigger Property dialog box as shown in Figs 4-12, 4-13, 4-14, and 4-15. The selected Trigger Position percentages will be displayed on the right side of the screen of the system.



Fig 4-12 - Trigger Position Pull-down Menu



Fig 4-13 – Trigger Position 0%

🕵 ZEROPLUS LAP-C	(16128) (S/	<b>W:00000</b>	00001) - [LaI	loc1]					
🌀 File Bus/Signal	. T <u>r</u> igger	Run/ <u>S</u> top	<u>D</u> ata <u>T</u> ools <u>W</u>	indow <u>H</u> elp					-181 ×
🗋 🖻 🖉 🕄	ii, 🔍 🖗	$\psi_{T}^{E}=\psi_{T}^{III}$	# 🔟 🕨 🕨		2K 🔽 🕯	∦∣л	n 100KHz 💽 🛲	- 10%	🔻 🐝 Page 🛛 1
🚯 🚯 🕅		N 🕅	🤭 🎞 🛛 🚟 👻	1.5625	% 🔽 👯	Bat		<u>le el [</u>	Heigh
Trigger Delay	1								
Scale:64		Displa	y Pos:0	A	Pos:805 -		A - T	= 805 👻	<u> </u>
Total:2048		Trigge:	r Pos:U	E	Pos:835 -		<u>B - T</u>	= 835 -	<u> </u>
Bus/Signal	Trigger	Filter	-1280	-960 -64	40 -320		320 640	<mark>960</mark>	1280 1600
🖌 🗛 🗛	x								
🖌 A1 A1									
🥖 A2 A2									
🧹 A3 A3									
<b>/ A4</b> A4			1		-	10%			

Fig 4-14 – Trigger Position 10%

🕵 ZEROPLUS LAP-C	(16128) (S/	/#:000000	00001) - [LaI	loc1]				_ 🗆 🗵
🌀 <u>F</u> ile B <u>u</u> s/Signal	T <u>r</u> igger	Run/ <u>S</u> top	<u>D</u> ata <u>T</u> ools <u>W</u>	indow <u>H</u> elp				_ 8 ×
🗋 🗅 😂 🔚 🎒	ii, 🛛 🖗	φ <sup>®</sup> <b>ΥΤ Υ</b>	🕅 🔝 🖉	> 🔲 🛛 🗟 alia 🛛 2K	▼ i♣i m 10i	OKHz 💌 🚥	- 70%	▼ 🔸 Page 1
🟠 😣 🔝 💌		N 🕅 🖇	🦻 🎬 🖉 👻	<b>.</b> 1.5625%			<u>]e e </u>	Heigh
Trigger Delay	1							
Scale:64		Display	y Pos:O	A Pos:	-424 🔻	A - T	= 424 💌	<u> </u>
Total:2048		Trigger	r Pos:O	B Pos:	-394 🛛 🕶	<u>B</u> - T	= 394 🔻	<b>.</b>
Bus/Signal	Trigger	Filter	-1280	-960 -640	1 <sub>320</sub>	320 540	960 1	280 1600
🖌 🖌 🗛	× •							
🖌 A1 A1								
<b>/ A2</b> A2								
🖌 A3 A3								
🖌 🗚 A4			1					
				70% -		30% —		

Fig 4-15 – Trigger Position 70%



#### Step6. Trigger Range Setup

Click **Trigger Property** from the Trigger on the Menu Bar. Then, Click the Trigger Range, the dialog box will appear as shown in Fig4-16.

**Tip**: This function is mainly for the range control for the saved files after triggering. According to the procedures of the range control, users can start the save of data according to the requirement of its time and times to get the standard of data statistic status.

Trigger Property	×
Trigger Content Trigger Delay Trigger Range	
🔽 Activate Trigger Range	
Range Setting	
Time Sample 🔽 1 minute	
OK Cancel Default Help	

Fig 4-16 - Trigger Range

1. Trigger Range : The default is not activated.

2. There are "Time Sample" and "Frequency Sample" in the part of Range Setting; the default is "Time Sample". The units of Time Sample are 'second', 'minute', 'hour' and 'day'. The unit of Frequency Sample is 'times'. Users can set the value by themselves in the editor box.

#### Task 3. Bus Trigger and Trigger Mark Setup

Step1. Click 👫 icon or click Bus Trigger Setup and Trigger Mark from the Trigger on the Menu Bar. The menu is shown as Fig 4-17.

$\widehat{\psi}_T^{B^{(i)}}$	Bus Trigger Setup
nn T	Channel Trigger Setup
.,∰	Trigger Property
İт	Trigger Mark
гд	Pulse Width Trigger Module(Option)
$\mathbb{Z}$	Don't Care
	Hi gh
	Low
25	Rising Edge
50	Falling Edge
X	Either Edge
	Reset

Fig 4-17 -Trigger Menu

Step2. Bus Trigger Setup

1. Bus Trigger Setup



Bus :	Trigger				×
Bus	: Trigger Pro	tocol Analyzer	Trigger		
	Bus Name	Operator	Value		
	Bus1	▼ =	▼ 3		
	-Data Format-				
	C Binary	🔿 Decimal	<li>Hexadecimal</li>	○ ASCII	
					_
		OK Car	ncel Defaul	.t Help	

Fig 4-18 - Bus Trigger Dialog Box

Tip: The Bus Name item can be selected from the pull-down menu (It only displays the general Bus name),

and also the ASCII mode is added.

2. Protocol Analyzer Trigger Setup

Bus Trigger		<u>&gt;</u>
Bus Trigger Protocol	Analyzer Trigger	
Allow Protocol A Protocol Analyzer	nalyzer Trigger Protocol Packet	Value
Busi (IIC)	<ul> <li>○ START</li> <li>○ ADDRESS</li> <li>○ READ</li> <li>○ WRITE</li> <li>○ A-ACK</li> <li>○ DATA</li> <li>○ D-ACK</li> <li>○ D-ACK</li> <li>○ D-ACK</li> </ul>	<ul> <li>▲</li> <li>Data Format</li> <li>○ Binary</li> <li>○ Decimal</li> <li>○ Hexadecimal</li> <li>▼</li> <li>◆ ASCII</li> </ul>
OK	Cancel	Default Help

Fig 4-19 - Protocol Analyzer Trigger

Allow Protocol Analyzer Trigger: When it is selected, the Protocol Analyzer Trigger function is activated. And then users can set Protocol Analyzer, Protocol Packet, Value and Data Format.

Protocol Analyzer: It only displays the name of Protocol Analyzer and only one name can be selected.

Protocol Packet: It is displayed according to the packet in every protocol analyzer.

**Value**: The value needs to be entered in the frame, and the data mode can be selected by users according to their requirements; the default is Hexadecimal! When a value can be input in the selected protocol analyzer data, the frame can be enabled! Or, the frame will be disabled! For example: Protocol Analyzer IIC, when the protocol packet is DATA, the frame can be used; to the contrary, when the protocol packet is START, the frame is disabled.

Data Format: The displayed value mode can be selected! There are four options: Binary, Decimal, Hexadecimal

#### and ASCII.

### Step3. Trigger Mark Setup

To find the item in the Bus better, users can activate the Trigger Mark function after starting Bus Trigger; the trigger mark is shown with T bar. According to the number of the trigger position, the T bar is displayed in order T0, T1, T2, T3, T4...and the color is red as the image below:

1. General Bus: The trigger condition is "0"; the red T bar displays the trigger condition in order.



Fig 4-20 - General Bus Trigger Mark

2. Protocol Analyzer (IIC): The trigger condition is "Data=0"; the red T Bar displays the trigger condition in order.

Bus/Signal	Trigger	Filter	-20		<b>3</b> -5 0 1			25
Bus1 (IIC)		⊗ -	0000	0000	oxoo 🛔	0000	0000	0X00
🖌 🖌 AD		$\otimes$						
🖌 A1 A1		$\otimes$						
<b>/ A2</b> A2		$\otimes$						
🥖 🗚 🕹		$\otimes$						
🖌 🗚 A4		$\otimes$						
🖌 A5 A5		$\otimes$						

Fig 4-21 - Protocol Analyzer Trigger Mark

### Task 4. Bus/Signal Trigger Condition Setup

Highlight a designated signal, and then set its required trigger condition.

- 1. Left click III to set the signal trigger condition as shown in Fig 4-22.
- 2. Right click to set the signal trigger condition as shown in Fig 4-23.
- 3. Click **Trigger** on the Menu Bar and choose a trigger condition from the list of triggers as shown in Fig 4-24.

			Bus/Signal	Trigger Filter -20
			🖌 🖌	right click
			<b>à1</b> à1	🚬 🐖 Bus Trigger Setup 🐺 🐺 Channel Trigger Setup
Bus/Signal	Trigger		• · · · ·	• Properties
🖌 🗛 AO		left click	🥖 A2 A2	Don't Care
🖌 A1 A1			<b>à4</b> à4	T Rising Edge
<b>/ A2</b> A2			•	Either Edge
			💉 A5 A5	Color
<b>/ A3</b> A3			🖌 🖌 A6	
🖌 🗚 A4			🖋 AT AT	
_		<b>—</b> .		



Fig 4-23 – Right Click on Trigger

Trigger Run/Stop Data Tools Window Help												
൙ Bus Trigger Setup												
🔐 Chan	<b>μ</b> γγ Channel Trigger Setup											
📲 Trig	📲 Trigger Property											
Trig	ger Mark											
🗖 Puls	🖵 Pulse Width Trigger Module(Option)											
🔀 Don'	t Care											
Hi gh												
Low												
🖍 Risi	ng Edge											
N Fall	ing Edge											
🔀 Either Edge												
Reset												

Fig 4-24 – Trigger Menu

### Task 5. Run to Acquire Data

### 1. Single Run

Click the Single Run icon from the Tool Bar or press **START** button on the top of the Logic Analyzer (or press F5), then activate the signal from the DUT to the Logic Analyzer to acquire the data shown in the waveform display area.

### 2. Repetitive Run

Click the Repetitive Run *icon* from the Tool Bar, then activate continuous signal to the Logic Analyzer to acquire the repetitive data, and then click the Stop *icon* to end the repetitive run.

Tip: Click 📓 icon to view all the data, and then select the waveform analysis tools to analyze the waveforms.

ZEROPLUS LAP-	C (32128) (S. al T <u>r</u> igger	/ <b>∦:000000-0000</b> Run/ <u>S</u> top <u>D</u> ata	) - [LaDo <u>T</u> ools <u>W</u> i:	ndow <u>H</u> ei	lp							
🗅 🗲 🖬 🎒	🔍 Z, 🂱	<b>∳</b> <sup>₽</sup> <b>₩ ₩</b>	3 • •		a 2K	• і∰і л	n 100Kł	iz 💌	ww	50%	▼ 🐝 F	age 1
🏠 🕓 🔝 🛛 🖻		k 🕅 🖑 🛅		1.96	078435 🔻	K Bar	Bar Bar	<b>T</b>	🎁 l4	<del>ک</del> ا ا		Heigh
Irigger Delay_ Scale:51 Total:2048		Display Pos: Trigger Pos:	1		A Pos:-1 B Pos:15	5   <b>~</b>   <b>~</b>		A B	- T = 1 - T = 1	5   <b>~</b> 5   <b>~</b>		<b>^</b>
Bus/Signal	Trigger	Filter	-1020	-765	-510 -	255	25	5 51	.0 7	65 I	07 .020 1	275
🖌 🗛 🗛	•	-										
🖌 A1 A1										******		
🥖 A2 A2						******				******		
🧭 A3 A3												
🖌 A4 A4												
🧪 A5 A5								1000			]	
🖌 🖌 A6				11			ЛЛ	$\prod$			]	
🖋 AT AT											]	
🖋 BO BO												
<b>B1</b> B1												

Fig 4-25 – Click 📓 Icon to View All the Data

### 3. Stop to end Run

Click the Stop <a>[</a> icon to end the Run.

**Tip:** If the status is "Waiting..." with no signal outputting as shown in Fig 4-26, click the Stop I icon to end the Run; check the setup again, and try the run process again.



Fig 4-26 - Waiting Status



# 4.2 Bus Logic Analysis

Section 4.2 presents detailed instructions about logic analysis with a set of grouped signals, which is known as Bus Logic Analysis.

Basic Software Setup of the Bus Logic Analysis

Step1. Set up the RAM Size, Frequency, Trigger Level and Trigger Position as described in Section 4.1.

Step2. Group signals into a Bus

Click **Channels Setup** on Bus/Signal of the menu bar, or click **2**, icon. The dialog box shown in Fig 4-27 will appear.



Fig 4-27 – Channels Setup

Rename the Bus and set up the channels of the Bus as shown in Fig 4-28.

Port				Por	tD			P	ort	Å			
Tr.Condition	$\mathbb{X}$	$\mathbb{X}$	$\mathbb{X}$		$\mathbb{X}$		$\mathbb{X}$	$\mathbb{X}$	$\mathbb{X}$	$\mathbb{X}$	$\mathbb{X}$		
Fi.Condition	$\mathbb{X}$		$\mathbb{X}$	$\mathbb{X}$	$\mathbb{X}$			X		X		X	
AO	7	6	5	4	3	7	6	5	4	3	2	1	0
A1	7	6	5	4	3	7	6	5	4	3	2	1	0
A2	7	6	5	4	3	7	6	5	4	3	2	1	0
Bus1	7	6	5	4	3	7	6	5	4	3	2	1	0
A4	7	6	5	4	3	7	6	5	4	3	2	1	0
A5	7	6	5	4	3	7	6	5	4	3	2	1	0
A6	7	6	5	4	3	7	6	5	4	3	2	1	0
A7	7	6	5	4	3	7	6	5	4	3	2	1	0
Assignment	1	1	1	1	1	3	3	3	1	1	1	1	1

Fig 4-28 – Rename Bus

- 1. Click the column with blue, then type the given name of the Bus, and then press Enter to confirm it.
- 2. Go to the relative channels as shown in the example and go to numbers 1, 2, 3, 4, 5 which are located on column A and row Bus1. Click them to become purple, then set these segments of channels.
- 3. Click **OK** to get the result as shown in area 1.


gy Co., Ltd

3	Bus/Si	gnal		Trigger H	/ilter		J.			-2	.0			▲ =1	5,			-10				5			1				5				1,0					
		<b>1</b> A1	0	Channels S	etup				_	_	-							_	-	_	_	_	-	_	-	_	_		-	-	-							×
								4	A	dd I	Bus/S	Sign	al		2	lete	Bus	/Sigi	nal	1		Del	ete /	411			Res	tore	Def	ault	5	ノ						
	🥖 A	<b>2</b> A2		Port					Por	t D						3	ort	С						P	ort	B						P	ort	A				•
		<b>9</b> 40		Ir. Condi	ition	X	X	$\times$	X	$\mathbb{X}$	X	$\mathbb{X}$	X	X	X	X	X	4	X	X	X	X	X	X	$\mathbb{X}$	$\times$	X	X	$\times$	X	X	X	$\mathbb{X}$	X	$\mathbf{X}$	X	$\supset$	•
	<u>,</u> ,	<b>U</b> NJ		Fi. Condi	tion		X	X	X	X	X	X	X		X		X	X	X	X		X		X	X	X	X		X	X	X	X		X				•
	— В	us1		A2		7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	ō	
		1		A3 Ruel		7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	
		🥖 AO .	AC	A4		7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	
				A5		7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	
		🥖 Å1 -	A:	A6 A7		7 7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	
		/ A2	A	Assignme		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	2	2	2	÷	<u>'</u>
				Lount		_	_		_				<u> </u>			_		_		<u> </u>												_	_	_	_	_		-
		🧭 🗚 .	<i>.</i>	🔽 Rese	rve wav	vefr	orm	data	a and	1 sh	nw h	hem	1.																									
		_	Ok Cancel Help											P																								
	4	<b>4</b> A4												-																								

Fig 4-29 - Channels Setup Window

#### Tip: Channels Setup

In the dialog box of Channels Setup, there isn't only Add Bus/Signal, but also Delete Bus/Signal, Delete All, Restore Defaults provided.

- 1. Delete Bus/Signal: Firstly highlight the Bus or channels on area 6 of Fig 4-29, then click Delete Bus/Signal to delete them.
- 2. Delete All; Click Delete All to delete all Bus/signals on area 6 of Fig 4-29.
- 3. Restore Defaults: Click Restore Defaults to restore the dialog box of Channels Setup as shown in Fig 4-27.
- Step3. Trigger Condition Setup
  - 1. Highlight the Bus which will be triggered then click 👎 icon or select Bus Trigger Setup from the Trigger of the Menu Bar, the dialog box as shown in Fig 4-30 will appear.

s Trigger			
Bus Trigger Pro	tocol Analyzer T	rigger	
Bus Name	Operator	Value	
Busi		▼ 1F	
-Data Format-			
C Binary	C Decimal	• Hexadecimal	O ASCII
	OK Canc	el Defaul	t Help

Fig 4-30 - Bus Trigger Setup

Tip: Double click on Trigger column of the Bus as shown in Fig 4-31.



Fig 4-31 – Trigger Column



- 2. Set Binary, Hexadecimal, Decimal or ASCII as the Data Format of the Bus to represent the value (see Fig 4-30).
- 3. Set "=" and "Don't Care", and type the value of the Bus into Value column to set the trigger condition of the Bus.
- 4. Click **OK** to confirm the settings.
- **Step4.** Click **Run** and activate the signal from the tested board to the system to get the result as shown in Fig 4-32.
  - **Tip:** Click icon to view all data, and then select the waveform analysis tools to analyze the waveforms. Set **Value** is "5E" as Hexadecimal, and set **Operator** equals to "=", then click **OK**. Click **Run** and

activate the signal from the tested board to the system to get the result as the trigger happens on 0X5E.

Signal	Trigger	Filter         -20         -15         -10         -5         5	10
	OX5E 🗸	■ • 0X46 0X5E	0X46
🖌 🖌 AC			
🥖 A1 A1		Bus Trigger Protocol Analyzer Trigger	
🥖 A2 A2		Bus Name Operator Value	
🧹 A3 A3		Busi V = V 5E	
🖌 🗚 Ad		O Binary O Decimal © Mexadecimal O ASCII	
🥖 A5 A5			
🖌 🖌 AB			
🖌 🖌 AT		OK Cancel Default Help	

Fig 4-32 – Bus Trigger Setup



# 4.3 Plug Analysis

### **Plug Introduction**

Protocol Analyzer operates in the form of Plug; every Protocol Analyzer has a plug, per plug is independence modularization. One Protocol Analyzer plug can analyze many Buses at the same time, however, because the independence of every plug, the Protocol Analyzer plug only supports IIC, UART, SPI, HDQ, 1-WIRE, CAN 2.0B at present. In the future, it will support more Buses, and when the Protocol Analyzer renews, it only needs to download the new Protocol Analyzer plug to cover the old Protocol Analyzer plug; the speed is very fast.

Operating Instructions: There are PlugIns data file in the position of installing LA software. All Protocol Analyzer plugs which are used at present are put in the data file, the DLL file can be added or deleted in the content, and in the Bus property, all Protocol Analyzer plugs that can be used at present can be seen as the figure below:

PluginsA		f. ×
Ain tot New Pevorts	s Tals Hep	(fl
4- teck - + - 1 Q	Search Carolines Carolines (Caroline X 20) 23-	
Address 🗋 PlugErsA		<u>▼</u> 2 <sup>2</sup> 58
PlugInsA Selet an ten to ven its description. See also: Hullenaments Hullenaments Hullenaments Hullenaments Hullenaments	nagiluite.d NagCullus RugeOg a RugeOd RugeOd RugeArt.di	



Bus Property	×												
General Bus Setting													
General Bus	Color Config												
Activate the Latch Function	A0 💌												
	Rising Analysis												
Protocol Analyzer Setting													
C Protocol Analyzer Parameters Config													
<ul> <li>ZEROPLUS LA IIC MODULE V1.08</li> <li>ZEROPLUS LA SM 2.0 MODULE V1.</li> <li>ZEROPLUS LA PM 1.1 MODULE V1.</li> <li>ZEROPLUS LA 3-WIRE MODULE V1</li> <li>ZEROPLUS LA HDQ MODULE V2.05</li> <li>ZEROPLUS LA I2C(EEPROM 24LX)</li> </ul>	Protocol Analyzer     Parameters Config     ZEROPLUS LA IIC MODULE V1.08     ZEROPLUS LA SM 2.0 MODULE V1.02     ZEROPLUS LA PM 1.1 MODULE V1.02     ZEROPLUS LA 3-WIRE MODULE V1.01     ZEROPLUS LA HDQ MODULE V2.05     ZEROPLUS LA I2C(EEPROM 24LX) MODULE V1.03												
🔽 Use the DsDp	Find												
More Protocol Analyzer: http://www.	.zeroplus.com.tw												
ОК	Cancel Help												

Fig4-34 - Bus Property



Every Logic Analyzer module supports some basic Protocol Analyzer plugs, for example: LAP-C(16032), LAP-C(16064) and LAP-C(16128) support IIC, UART Protocol Analyzer plugs; LAP-C(32128), LAP-C(321000) and LAP-C(322000) support IIC, UART, SPI Protocol Analyzer plugs. However, LAP-C(16032), LAP-C(16064) and LAP-C(16128) don't support SPI Protocol Analyzer plug, when users need to use this analysis, they can purchase from our company, and then, they can get SPI Protocol Analyzer plug and the register code.

STEP 1. Put the SPI Plug in the PlugIns as the Fig4-35.



Fig4-35 - PlugInsA

STEP 2. Select SPI in the Protocol Analyzer list.

Bus Property	×											
General Bus Setting												
O General Bus	Color Config											
Activate the Latch Function	A0 💌											
	Rising Analysis											
Protocol Analyzer Setting  Protocol Analyzer Parameters Config												
☑ Use the DsDp	Find											
More Protocol Analyzer: http://www OK	Cancel Help											

Fig4-36 - Bus Property

STEP 3.Click Parameters Configuration button, select Register and use SPI for free.

Use SPI for free!	
instructions below. Our te questions you have. >> By phone:	chnical support team will be happy to answer any Tel:886-2-66202225
	Mail : service 20zeroplus.com.tw
// ADDIICations through E	······
>> Website:	http://www.zeroplus.com.tw
<pre>&gt;&gt; Applications through E &gt;&gt; Website: Copyright(C) 1997-2009 ZE</pre>	http://www.zeroplus.com.tw RROPLUS TECHNOLOGY CO.,LTD.

Fig4-37 - Protocol Analyzer SPI Setup



# 4.4 Bus Packet List

Bus Packet List is a graphics list which is used for doing Statistics and showing Bus Packet List. It is visual and direct, especially for IIC, USB and CAN 2.0B. When there is a packet list, it gets twice the result with half the effort to check the data. Packet List has its startup button in Toolbar. After starting it, it will show a small window under the waveform window. Users can alter its size to find more data.



🗊 ZEROPLUS LAP-C (321)	28) (S/X:000	000-0000) ·	- [LaD	oc1]									_ 🗆 ×
ዀ <u>F</u> ile B <u>u</u> s/Signal T <u>r</u>	igger Run/ <u>S</u> t	op <u>D</u> ata <u>T</u> o	ols <u>W</u> i	ndow <u>H</u> ei	lp								_ 8 ×
🗅 差 🖬 🎒 🔍 9	🤅 💱 🥐 🖗	r "🗉 🔟	D DD	• 🔲 🔤	4 2K	▼   ↓↓	<b>n</b> 10	OKHz	vuu 👻		%	Page	1 🔹
🚯 😣 🗟 📰		) 🖑 🗰 🛛	* ,	ي 125.	490191	- MU		B <mark>⊻ T⊮</mark> : Bar Bar I		]∳ ¢[	8US	Ap He	ight <b>40</b>
Trigger Delay 1													,
Scale:0.796875	Display	Pos:O		A Pos:-	15 🔻		A -	T = 15	-		A - B =	30 🔻	
Total:2048	Trigger	Pos:O		B Pos:1	5 🗸		в -	T = 15	<b>-</b>		Compr-F	late:No	
Bus/Signal Tri	igger Filte	er 🗧 💷	A 15.938	-11.953	-7.969	-3.9	84		984 7	. 96 9	11.953	B 15.938	19,922
Bus1	× • ×		XXX	XXXX	XXX	000	000	XXX		000	)))(		2000(-
<b>ad</b> ac			Ш	Л	$\square$					$\Box$			
🖌 🗚 🗛													
<b>/ A2</b> A2													
<b>/ A3</b> A3													
A4 A4													
Setting Refresh	Export S	ynch Parametei	r										
Packet # Na	me T	imeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length
1 Bus1(G	ieneral)	-1023	0X0	0X1	0X2	0X3	OX4	0X5	0X6	0X7	0X0	0X1	
Packet # Na	me T	imeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length
2 Bus1(G	ieneral)	-1013	UX2	UX3	UX4	UX5	UX6	UX7	UXU	UX1	UX2	UX3	10
Packet # Na	me T	-1002	Data	Data	Data	Data	Data	Data ovi	Data	Data	Data	Data	Lengtr
Busile	mo T	-1003	Data	Data	Data	Data	Data	Data	Data	Data	Doto	Data	
4 Bus1/G	eneral)	-993	Data DX6	OX7	OX0	OX1	OX2	OX3	OX4	OX5	OX6	OX7	10
		· •	-										
Ready											End!		DEMO

Fig 4-38 - Packet Icon



Packet List has a setup window; users can set up the Packet List according to their requirements. Setting General Bus Packet Length in dialog box is only used for doing General Bus Statistic. Users can define how long the time is as a data packet to add the export function. See the following figure.



Setting	X
Bus Select	Data Format
☑Bus1(General)	◯ Bin ◯ Dec . ● Hex ◯ ASCII
	General Bus Packet Length
	10 Min: 1 Max: 2048
Color	
Packet Name	TimeStamp Length Data
Text	C Text Color Auto
OK.	Cancel Default Help

Fig4-40 - Packet List Setting

BUS Packet	List											×			
Setting	Setting Refresh Export Synch Parameter														
Packet #	Name	TimeStamp	Data												
1	Bus1(General)	-1023	0X0	0X1	0X0	0X1	0X0	OX1	0X0	OX1	0X0				
Dat OX	ta Length 1 10														
Packet #	Name	TimeStamp	Data												
2	Bus1(General)	-1013	0X0	0X1	0X0	0X1	0X0	0X1	0X0	0X1	0X0				
	ta Length 1 10														
Packet #	Name	TimeStamp	Data												
3	Bus1(General)	-1003	0X0	0X1	0X0	0X1	0X0	OX1	0X0	OX1	0X0				
Dat	ta Length											-			

Fig4-41 - General Bus Packet List

1. View Specifications

Packet #, Name and TimeStamp are the fixed items.

Packet #: List the order of Packet.

Name: Display the name of Packet, or the Filter Display Bar.

**TimeStamp:** It is the starting point of the Packet.

Tip: The rest name and content are supplied by Plug.

BUS Packet	List							×
Setting	Refresh Expor	t Synch P	arameter					
Packet #	Name	TimeStamp	ADDRESS	READ	A-NACK	Describe		-
1	IIC BUS(IIC)	477	0X7F	READ	A-NACK	ADDR NACK		
Packet #	Name	TimeStamp	ADDRESS	READ	A-NACK	Describe		
2	IIC BUS(IIC)	5231	0X7F	READ	A-NACK	ADDR NACK		
Packet #	Name	TimeStamp	ADDRESS	READ	A-NACK	Describe		
3	IIC BUS(IIC)	9165	0X7F	READ	A-NACK	ADDR NACK		
Packet #	Name	TimeStamp	ADDRESS	READ	A-NACK	Describe		
4	IIC BUS(IIC)	16367	0X7F	READ	A-NACK	ADDR NACK		
Packet #	Name	TimeStamp	ADDRESS	READ	A-NACK	Describe		
5	IIC BUS(IIC)	20290	0X7F	READ	A-NACK	ADDR NACK		-

Fig4-42 - Protocol Analyzer IIC Packet List

Setting: It is used to open Packet List Setting dialog box.



Refresh: Press this button, the list view can renew automatically.

Export: Export the workspace into Text (\*.txt) and CSV Files (\*.csv).

**Synch Parameter:** Open the synch parameter setting dialog box and activate the packet and waveform synch function.

2. Display Protocol Analyzer Packet in Order

Tip: The below view are Protocol Analyzer IIC; the packet is determined by the position of the TimeStamp.

BUS Packet	List							×
Setting	Refresh Expo	rt Synch P	ara	ameter	]			
Packet #	Name (	TimeStamp	A	DRESS	READ	A-NACK	Describe	
1	IIC BUS(IIC)	477		OX7F	READ	A-NACK	ADDR NACK	
Packet #	Name	TimeStamp	A	DRESS	READ	A-NACK	Describe	
2	IIC BUS(IIC)	5231		OX7F	READ	A-NACK	ADDR NACK	
Packet #	Name	TimeStamp	A	DRESS	READ	A-NACK	Describe	
3	IIC BUS(IIC)	9165		OX7F	READ	A-NACK	ADDR NACK	
Packet #	Name	TimeStamp	A	DRESS	READ	A-NACK	Describe	
4	IIC BUS(IIC)	16367		OX7F	READ	A-NACK	ADDR NACK	
Packet #	Name	TimeStamp	A	DRESS	READ	A-NACK	Describe	
5	IIC BUS(IIC)	20290		0X7F	READ	A-NACK	ADDR NACK	-

Fig4-43 - TimeStamp

**Tip:** When the Display Bar of Signal Filter is activated, the Bar should be displayed in the Bus Packet List, and also the TimeStamp, ADDRESS and length of the Bar will be displayed.

3. Packet Idle and Packet Length

Packet Idle: Packet interval time Packet Length: Packet time length

When those above two items are to be displayed, it only chooses one of them to display, which is controlled by Plug.

Because it is impossible that every Protocol Analyzer packet has registered timestamp and end, we add two special Unknow\_Flag to judge the timestamp and end of the packet which are Unknow \_Start\_Flag and Unknow\_End\_Flag.



Fig4-44 - Protocol Analyzer IIC Packet Length

Tip: Because IIC has started as the Packet TimeStamp, it does not need to use Unknown\_Start\_Flag as the start.

4. General Bus



	100 0												
li	iUS Fac	ket L	ist										Ä
	Setting.	Re	efresh	Export.	Syr	nch Para	meter						
1	Parke	+ #		Namo		Time	Stamp	Data	Data	Data	Data	Data	▲
	1	1 Bust (General)		-1023			011		011				
ľ	1	Data	Data	Data	Data	Data	Longth		0/1	0/10	OAT	0/10	)
	Data		Data	Data	Data	Data OX1	Lenger	-					
I.		UXI	0.00	UXI	0.00	UXI			_				
	Packe	et #		Name		Time	eStamp	Data	Data	Data	Data	Data	
l	2	2 Bus1(General)		ral)	-1013		OXO	0X1	0X0	0X1	OXO	ļ	
	Data		Data	Data	Data	Data	Length						
		OX1	0X0	0X1	0X0	0X1	10	7					
	Packe	:t#		Name		TimeStamp -1003		Data	Data	Data	Data	Data	
	3		Bust	1(Gene	ral)			0X0	0X1	0X0	0X1	0X0	
ľ		Data	Data	Data	Data	Data	Length						, 
		0X1	0X0	OX1	0X0	0X1	10						
l	Packe	:t#		Name		Time	eStamp	Data	Data	Data	Data	Data	
ľ	4		Bus	1(Gene	ral)	-	-993		0X1	0X0	0X1	0X0	
ľ		Data	Data	Data	Data	Data	Length						
		0X1	0X0	OX1	0X0	0X1	10						
I	Packe	:t#		Name		Time	eStamp	Data	Data	Data	Data	Data	
1	5		Busi	1/Gene	rah	-	983	0X0	0X1	OXO	0X1	OXO	-

Fig4-45 - General Bus Packet List

#### Packet Length and Packet Idle Length

Packet's TimeStamp is the start of Bus Data; the default length is controlled by the setting dialog box. If the input packet length isn't the end of data. The software will prolong the length of Packet to end the data automatically as the figure below.





The Fig4-46 is a General Bus; its first data is 0x00, and its length is 1023. If users input 20 as the General Bus length. But 20xaddress is not the end of this data, so the software will prolong the length of the Packet to 1023 automatically.



Fig4-47 - Packet End

The Fig4-47 is a General Bus. If the Start of the packet is T bar and the set General Bus length is 20, but the data 0x02 isn't the end, at that time, the Packet will be prolonged to the end dot automatically, that is to say, the Address

27 (B bar ) is the End of the packet.

The above two data are made consecutively as the figure below.



Fig4-48 - Auto-Prolong Packet

The Packet List is displayed as the figure below:

BUS Packet L Setting R	ist efresh	Export	Syr	nch Para	meter						×
Packet #	Bus	Name 1(Gene	ral)	Time	eStamp 1023	Data 0X0	Data 0X1	Data 0X0	Data 0X1	Data 0X0	
Data OX1	a Data Data Data 1 0X0 0X1 0X0		Data 0X1	Length	]						
Packet # 2	Name Bus1(General)			Time -1	eStamp 1013	Data 0X0	Data 0X1	Data 0X0	Data 0X1	Data 0X0	
Data 0X1	Data 0X0	Data 0X1	Data 0X0	Data 0X1	Length 10						
Packet # 3	Name Bus1(General)		Time -1	TimeStamp -1003		Data 0X1	Data 0X0	Data 0X1	Data 0X0		
Data 0X1	a Data Data Data 0X0 0X1 0X0		Data 0X1	Length 10							
Packet # 4	Name Bus1(General)		Time	TimeStamp -993		Data 0X1	Data 0X0	Data 0X1	Data 0X0		
Data 0X1	a Data Data Data . 0X0 0X1 0X0		Data 0X1	Length 10							
Packet # 5	Name Bus1(General)			Time	TimeStamp -983		Data 0X1	Data 0X0	Data 0X1	Data 0X0	-

Fig4-49 - General Bus Packet List

Tip: The Protocol Analyzer Packet will be explained in the following plug.

5. Packet and Waveform Synchronization

For the convenience of fast corresponding between packet data and waveform data, and what is more, in order to make it easier for users to look up data, we add the Packet and Waveform Synchronization function.

In order to operate conveniently, we add a Synch Parameter button on the BUS Packet List as the image below:

BUS Pac	ket L	ist		_			<b>`</b>					×
Setting.	Re	efresh	Export.	. Syr	nch Parai	meter	J					
Packe	et #		Name		Time	eStamp	Data	Data	Data	Data	Data	-
1		Bust	1(Gene	ral)	-1	.023	0X0	0X1	0X0	0X1	0X0	
	Data	Data	Data	Data	Data	Length						
	0X1	0X0	0X1	0X0	0X1	10						
Packe	et #		Name		Time	eStamp	Data	Data	Data	Data	Data	
2		Bus1(General)			-1	.013	0X0	0X1	0X0	0X1	0X0	
	Data	Data	Data	Data	Data	Length						
	0X1	0X0	0X1	0X0	OX1	10						
Packe	et #		Name		Time	TimeStamp		Data	Data	Data	Data	
3		Bus1(General)		-1	-1003		OX1	0X0	0X1	0X0		
	Data	Data	Data	Data	Data	Length						
	0X1	0X0	0X1	0X0	OX1	10						-

Fig 4-50 - Synch Parameter on the BUS Packet List

At the same time, a Synch Parameter Setting dialog box is added.



Synch Parameter Setting	X
Activate Packet and Waveform	Synch
Synch Point of Packet List	Synch Point of Waveform Area
• Тор	O Left
O Middle	<ul> <li>Middle</li> </ul>
	OK Cancel

Fig 4-51- Synch Parameter Setting Dialog Box

Activate Packet and Waveform Synch: The default is not activated.

**Top**: When the Packet and Waveform Synch is activated, the synch point in Packet List is the top packet segment which is displayed by list.

**Middle**: When the Packet and Waveform Synch is activated, the synch point in Packet List is the middle packet segment which is displayed by list.

**Left**: When the Packet and Waveform Synch is activated, the synch point in the waveform area is the left packet segment which is displayed by waveform.

**Middle**: When the Packet and Waveform Synch is activated, the synch point in the waveform area is the middle packet segment which is displayed by waveform.

Activate Packet and Waveform Synch, select Top and Left.

Synch Parameter Setting	×
✓ Activate Packet and Waveform	Synch
- Synch Point of Packet List	Synch Point of Waveform Area
🕫 Тор	• Left
O Middle	O Middle
	OK Cancel

Fig 4-52 - Synch Parameter Setting Dialog Box



Display the corresponding waveform and packet as below image:

	•		•			·				•				
🕵 ZEROPLUS LAP-C	(16128) (S	/#:00000	0-0000)	- [IIC. (	uls]								_	
🋵 <u>F</u> ile B <u>u</u> s/Signal	. T <u>r</u> igger	Run/ <u>S</u> top	<u>D</u> ata <u>T</u>	ools <u>W</u> in	dow <u>H</u> el <sub>l</sub>	P							_	BN
🗋 🗅 😂 🖥 🎒	亂 🔍 鞭	₩ YT ·	• <sup>30</sup>   👿	D DD	■ <b>M</b>	128K	▼ (♣)	10MH	lz ▼	ww.	50%	🕶 🔸 Pag	e  1	•
🚯 🚯 🔝			🖤 🗰 📗	×	6.25%	6 🔻			Tr +2	<b>1</b> 4	\$া 😿	EUS 🔶 I	leight	40
Trigger Delay	1													,
Scale:16	D	isplay Pos	:: 1011		A Pos:-64	4527 🔻		A - T	= 64527	•	A -	B = 30 🖛		
Total:131072	Т	rigger Pos	::0	1	B Pos:-64	4497 🔻		B - T	= 64497	•	Comj	pr-Rate:No		
Bus/Signal	Trigger	Filter	<u>.</u>	6.91	771	851	931	1011	1091	1171	1251	1331	1411	<b>_</b> _
Busi (IIC)	-			C	X6E	F	READ	A-A	ACK D	ATA :	0X25	5		
🖌 🖌 AO	×													_
🖌 🖌 A1														
🥖 A2 A2														
🧭 A3 A3			-											
▲▲ ▲▲ ▲▲	│ <u>⋈</u>     ) •	■   →	1					Γ						•
× Setting Refree	sh Export	Synd	h Paramete	er										
Packet # N	Name	TimeStarr		RESS RE	AD A	-ACK	DITA	D-ACK	DATA	D-ACK	DATA	D-ACK	DATA	-
1 Bu	s1(IIC)	31	OX	ige Re	AD A	-ACK	0,25	D-ACK	0X36	D-ACK	0X47	D-ACK	0X58	
D-ACK	DATA	D-ACK	DATA	D-ACK	DATA	D-ACK	DATA	D-ACK	DATA	D-ACK	DATA	D-ACK	DATA	
D-ACK	0X69	D-ACK	0X7A	D-ACK	OX8B	D-ACK	0X9C	D-ACK	OXAD	D-ACK	OXBE	D-ACK	OXCF	
D-ACK D-ACK	DATA OXE0	D-ACK D-ACK	DATA 0XF1	D-ACK D-ACK	DATA 0X02	D-ACK D-ACK	DATA 0X13	D-ACK D-ACK						
Packet # M 2 Bu	Vame Is1(IIC)	TimeStam 17037	np ADDF OX	RESS RE	AD A	-ACK -ACK	DATA 0X49	D-ACK D-ACK	DATA 0X5A	D-ACK D-ACK	DATA 0X6B	D-ACK D-ACK	DATA 0X7C	
		5 1 OV			0. T	- 1 AV	Lour.				1.0.0		<b>-</b>	_
Ready											End		DEMO	11.

Fig 4-53 - Waveform and Packet Synchronization Interface



# 4.5 Bus Analysis

The setup is correlated to the Bus which needs to be made up, for example: General Bus, Protocol Analyzer. Open the dialog box:

STEP 1.Click Tools on the Menu Bar, and then select **Bus Property** or select **bus** to set up Bus Property.



Fig4-54 - Bus Property on Menu Bar

Fig4-55 - Bus Property on Tool Bar

STEP 2.Click the Right Key on the Bus/Signal column, and then select Bus Property.

Tip: The signals must be grouped into Bus, or the Bus Property can not have effect.



Fig4-56 - Right Key to Set Bus Property



## 4.5.1 General Bus Analysis

The General Bus Analysis function enables the system to analyze the General Bus.

Basic Software Setup for the General Bus

STEP 1. Click **Bus Property**, the following dialog box will appear.

D sing Analysis S Parameters Config
sing Analysis
Parameters Config
Parameters Config
DULE V1.03

Fig4-57 - General Bus Setting

STEP 2. Click **Color Configuration** to set Bus data color.

General Bus	Color Config
Activate the Latch Func	tion A0
	Rising Analysis
Protocol Analyzer Setting	
_	
Protocol Analyzer     ZEROPLUS LA 3-WIRE MO     ZEROPLUS LA HDQ MODL	DDULE V1.01 JLE V2.05
Protocol Analyzer C ZEROPLUS LA 3-WIRE M( ZEROPLUS LA HDQ MODU C ZEROPLUS LA IZC(EEPRO ZEROPLUS LA IZC(EEPRO ZEROPLUS LA IZC(EEPRO ZEROPLUS LA MODUI ZEROPLUS LA SM 2.0 MO ZEROPLUS LA SPI MODUI	Parameters Config DDULE V1.01 JLE V2.05 DM 24LX) MODULE V1.03 .E V1.08 DDULE V1.04 DDULE V1.02 LE V1.10

Fig4-58 - Color Configuration



Bus Data Color			×
Bus Name: Bus1			
Data Condition:	Data Min:	Data Max:	
= 💌	0	F	
Select Color:			
	ОК	Cancel H	ielp

Fig4-59 - Bus Data Color

**Bus Name:** Display the selected Bus name.

**Data Condition:** Select the Data Condition to change the Bus data color. There are four options which are = , !=, In Range and Not In Range.

Data Min.: Enter the min. data that is required by users.

**Data Max.:** Enter the max. data that is required by users. The max. data can be used only when the set is In Range or Not In Range.

Select Color: Select the changed color according to the Bus condition set by users.

STEP 3. Click **Color Configuration** to open the Bus Data Color dialog box, and set the "Data Condition = 0" and Select Color is Orange.

Bus Name: Bus1	
Data Condition: Data Min:	Data Max:
Select Color:	Cancel Help
Fig4-60 - Set the Color for	Bus1

15/Signal	Trigger	Filter		-20	-15	-10		·5		5		1	5
<mark>Bus1</mark>		-	0 <mark>X</mark> 2	) OX3	(oxo)	(OX1)	OX2	(OX3)	(oxo)	(OX1)	(0X2)	(ox3)	OXO
🖌 🖌 AC													

Fig4-61 - Before the Bus Data Color Setting

Bus/Signal	Trigger	Filter		-20	-15	-10	-	-5 	, <b>,</b> , ,	5	10	1	.5
Busl	-	-	0 <mark>X</mark> 2	(OX3	OXO	(OX1)	(0X2)	(OX3	OXO	OX1	OX2	(ox3)	OXO
🖌 🔥 AC													

Fig4-62- After the Bus Data Color Setting

**Tip:** Reserve the original state by the above steps.

2. Activate the Latch function

Activate the Latch Function: The default is not activated. When the Latch function is activated, the default channel is A0, and there are three conditions for selecting, Rising Analysis, Falling Analysis and Either Analysis; the default is Rising Analysis.

Set the Latch function for one Bus. The setting of the Latch channel is A0; the analysis function adopts Rising

Analysis.

us Property	×
General Bus Setting	I
C General Bus	Color Config
Activate the Latch Function	A0 💌
	Rising Analysis
Protocol Analyzer Setting	
O Protocol Analyzer	Parameters Config
C ZEROPLUS LA 3-WIRE MODULE VI	.01
C ZEROPLUS LA HDQ MODULE V2.05	
C ZEROPLUS LA IZC(EEPROM 24LX) I	MODULE V1.03
C ZEROPLUS LA IIC MODULE VI.08	04
C ZEROPLUS LA SM 2 0 MODULE V1.	02
C ZEROPLUS LA SPI MODULE V1.10	
Use the DsDp	Find
More Protocol Analyzer: http://www.	zeroplus.com.tw
Hore Hoteler Hildyzer Heepijji	
OK	Cancel Help

Fig4-63 - Activate the Latch Function

The picture of the waveform analysis:

🐝 ZEROPLUS LAP-C	(32128) (S	/₩:000000	-0000) - [LaDoc	u						
🋵 File Bus/Signel	Trigger	Run/Stop	Data Tools Mind	ow <u>H</u> elp						X
	略 統 響	** ** •		2K	■ 1401 100 1	00KHz 💌 🚥		Page 1	▼ Count 1	<u>▼</u> å å
🏠 🕓 🔝   🖾		R 📓 🤇	🦻 🎬 🛛 🖼 👻	333.333333: -		Be Te ter	i le 🌖 🔯 💾	Height	40 - Trigg	er Delay 1
Scale:0.3 Totel:2048		Disp	lay Pos:0 ger Pos:0	A P B P	os:=15   <del>•</del>		A - T = 15 -		A - B = 30 v	
10000			<b></b>		04.10				ompt nations	
Bus/Signal	Trigger	Filter	-6	-4.5	-3	-1.5	0 1, 5		4.5	6
Busi	$\boxtimes$	$\boxtimes$	1011	11	L01	0001	0011	0101	0111	1001
🖌 🖌 AD AC		×								
🖌 🖌 Al										
🖌 A2 A2		×								
🖌 A3 A3	$\boxtimes$	×								
🖌 A4 A4		$\boxtimes$								
🖌 AS AS		$\otimes$								
🖌 🗚 A6		$\boxtimes$								
🖋 AT AT										
🖋 BO BO										
🖌 B1 B1		$\otimes$								
<b>/ B2</b> B2	×	×								
<b>/ B3</b> B3										
<b>▲ B4</b> B4			T							T T
Ready									End	DEMO

Fig4-64 - The Latch Function Displayed on the Waveform Area

Illustration: The selected channel is A0; the analysis mode is Rising Analysis; it indicates that the data of the A0 is read at the Rising Edge. Seeing the T Bar in the above figure, the data of Bus1 is 0011.



## 4.5.2 IIC Analysis

### **IIC Introduction**

The IIC, which stands for Inter-Integrated Circuits, is a serial synchronous half-duplex communication protocol. The IIC was first proposed by Philips Semiconductor Netherlands. This IIC protocol consists of a very simple physical interface which has only two signal channels, SDA (Serial Data) and SCL (Serial Clock). Most IIC devices consist of an independently sealed IIC chip, and this IIC chip has direct connection to both SDA and SCL. The data transmission is a byte-base (8-bit base) for every segment. Since many oscilloscopes do not allow engineers to observe timing sequence information directly from the screens of oscilloscopes, this Logic Analyzer was created to help engineers resolve timing sequence issues during their circuit development.

IIC has a multi-control Bus as its physical and firmware interfaces. This protocol analyzer is basically a signal network that may connect to one or several control units. The intention of inventing this protocol was in the application of designing television sets, which allowed the central processing unit to quicken data communications with peripheral chips and devices. The IIC interface is initiated with a SDA triggered **High** and SCL triggered **Falling Edge**. Following the initiation, there will be a set of 7 bits (or 10 bits) address space. Beyond this point, there will be Read/Write, ACK (Acknowledgement), and STOP (or HALT/HLT). The signal information packet is transmitted in bytes. If there are two or more devices trying to access the IIC protocol, whichever device has SCL at logic high will gain access priority.

Furthermore, since IIC is a synchronous communication protocol and data transmission must be in bytes, a complete IIC signal packet must consist of **START**, **ADDRESS**, **READ/WRITE**, **DATA**, **ACK/NACK**, and **STOP** segments. They are as following.

START:	This is the initiation of SCL and SDA (1 bit only).
ADDRESS:	This identifies the device address (7 bits).
READ/WRITE:	This is a data direction bit. 0 = Write, 1 = Read.
ACK/NACK:	This is a confirmation bit following every data transmission segment.
DATA:	The actual signal data transmitted by byte.
STOP:	This appears when SCL = High and SDA = Low (1bit only).





## 4.5.2.1 Software Basic Setup of Protocol Analyzer IIC

- Step1. Set up RAM Size, Frequency, Trigger Level and Trigger Position as described in Section 4.1.
- **Step2.** Set up the Falling Edge as the trigger condition on the signal which connects to the tested IIC data pin (SDA).
- Step3. Group the analytic channels into Bus1.



Fig4-65 - Group into Bus

Step4. Select Bus 1, then, press Right Key on the mouse to list the menu. Next, click Bus Property or click Tools and the select Bus Property or click to open Bus Property dialog box.



Fig4-66 - Bus Property

Step5. For Protocol Analyzer Setting, select Protocol Analyzer. Then, choose ZEROPLUS LA IIC MODULE V1.08. Next, click Parameters Configuration. The following image will appear.



孕龍科	技股份	有限公司	3
Zeroplus	Technole	ogy Co., Lt	d.

PROTOCOL ANALYZER I	IC SETUP:Bus1			×
Configuration Timin	g   Packet   Regis	ter		
Pin Assignment Protocol Analyzer	Nam: Busl	SDA : AO	SCL :	A1
-Protocol Analyzer	Setting			
Custom Setti	ng			
-Protocol Analyzer	Color			
START	DATA	ADDRESS	READ	WRITE
A-ACK	A-NACK	D-ACK	D-NACK	STOP
		OK C	ancel Defa	ult Help

Fig 4-67 – Protocol Analyzer IIC Setup

#### Step6. Set the Pin Assignment.

- 1. Pin Assignment : Set the display name of IIC in Bus1.
- 2. SDA: Choose SDA channel for IIC
- 3. SCL: Choose SCL channel for IIC
- **Tip:** It is recommended that SDA and SCL channels are named as SDA and SCL to help distinguish them. 4. Protocol Analyzer Color: Set colors of the segment in the protocol analyzer.
- Step7. Click Custom Setting to define the IIC Data to meet users' requirements. The dialog box as shown in Fig 4-68 will be displayed.

Protocol Analyzer Customize		×
Read / Write bit Active Read Bit Conditions G High C Low Write Bit = Low	Data Area Contents Address Data Name: ADDRESS DATA Number of Bit: 7 222	OK Cancel Default
Ack Bit PlugIIC	×	
Ack Bit Condition	ust be between 1 and 28	

Fig 4-68 - Inputting Data Bits

1. Read/ Write Bit Setup:

Click on "Active" to set the segment of Read/ Write Bit in the Protocol Analyzer IIC, then select "High" or "Low" to set the condition of the Read/ Write Bit for the DUT.

Click off "Active" to remove the Read/Write Bit segment from the Protocol Analyzer IIC.

2. Ack Bit Setup:

Click on "Don't Stop Analysis when NACK happens" to continuously analyze the signals when the system says NACK Bit, then select "High" or "Low" to set the condition of the NACK Bit for the tested Protocol Analyzer IIC.

Click off "Don't Stop Analysis when NACK happens" to stop analyzing the signals when the system reads NACK Bit.

3. Give the names and the numbers of Bits to the Address Bit and Data Bit on the columns located in Data area for the tested Protocol Analyzer IIC.

The range for "Number of Bit" is from 1 to 28 bits.

4. Click on "Address left shift one bit then AND Read/Write Bit" to have an additional 1 bit on the right side of the Address Data content.



- 5. Press "OK" to confirm the setup of IIC Custom Setting and return to Protocol Analyzer IIC Setup dialog box. (**Tip:** Press "Default" to give up the current setup)
- **Step8.** Press **OK** to exit the dialog box of Protocol Analyzer IIC Setup.
- Step9. Click Run to acquire IIC signal from the tested IIC circuit. Refer to Fig 4-69.
- Tip: Click the IIC icon, then press "Stop" to exit IIC analysis mode.
- Tip: Click 📓 icon to view all data, and then select the waveform analysis tools to analyze the waveforms.



Fig 4-69 - Waveform Analysis





## 4.5.2.2 Protocol Analyzer IIC Timing Analysis

Fig 4-70 – Protocol Analyzer IIC Timing Setup

Waveform Image: Describe the position of the setting time.

**Time Format Settings**: When the Time Settings are activated, the set time will become the condition to judge the decoding. For example, when you want to decode START, you should judge whether the conditions of START is satisfied firstly, and then judge whether the set time of tHD: STA is suitable for the factual waveform; if the two conditions are satisfied, the START could be decoded; the theory of START decoding is the same to that of other packet segments.



## 4.5.2.3 Protocol Analyzer IIC Packet Analysis

PROTOCOL ANALYZER II	C SETUP:Bus1			×
Configuration   Timing	Packet Register			
Item	Color	Item	Color	
ADDRESS		A-NACK		
🔽 READ		🔽 D-ACK		
VRITE		🔽 D-NACK		
🔽 DATA		V DESCRIBE		
A-ACK				
	OK	Cancel	Default Help	

Fig4-71 - Protocol Analyzer IIC Packet Setup

ADDRESS: Start bit address or time display

**READ:** Read field displayed in packet

WRITE: Write field displayed in packet

A-ACK/A-NACK: A-ACK field has 2bit in all. If it receives successfully, it sends back "0" and "1". If it isn't "0"

and "1", it displays "A-NACK".

DATA: List the data field captured signal by Bus in the packet display.

D-ACK/D-NACK: D-ACK has 2bit in all.If it receives successfuly, it sends back "0" and "1". If it

isn't "0" and "1", it displays "D-NACK".

DESCRIBE: Error description to any field (format or data bit)

It is a Bus Packet List view, which includes 4 formats, which IIC happens as follows.

BUS Pac	ket	List									×
Setting.		Refres	h E:	kport Syr	nch Parame	ter					
Packet	#	Nar	ne	TimeStamp	ADDRES	S WRITE	A-ACK	DATA	D-AC	K	<b>_</b>
1		Bus1	(IIC)	611	OX3B	WRITE	A-ACK	0X12	D-AC	ĸ	
Packet	#	Nar	ne	TimeStamp	ADDRES	S READ	A-ACK	DATA	D-ACK	DATA	
2		Bus1	(IIC)	86209	0X34	READ	A-ACK	0X89	D-ACK	0X78	
	D	-ACK	DAT.	A D-ACK	DATA	D-ACK					
	D	-ACK	0X63	7 D-ACK	0X56	D-ACK					
Packet	:#	Nar	ne	TimeStamp	ADDRES	S WRITE	A-NAC	IK De	escribe		
3		Bus1	(IIC)	226891	OX3B	WRITE	A-NAC	ж ade	R NACK		
Packet	:#	Nar	ne	TimeStamp	ADDRES	S READ	A-ACK	DATA	D-ACK	DATA	
4		Bus1	(IIC)	294656	0X34	READ	A-ACK	0X89	D-ACK	0X78	
	D	-ACK	DAT.	A D-ACK	DATA	D-NACK	Descrit	oe 👘			
	D	-ACK	0X63	7 D-ACK	0X56	D-NACK	DATA N/	ACK			
											_
1											

Fig4-72 - Protocol Analyzer IIC Packet List



Packet1: It is commonly normal data, which includes 1 "ADDRESS" and 1 "DATA".

Packet2: It is commonly normal data, which includes 1 "ADDRESS" and 4 "DATA".

Packet3: The data includes 1 "ADDRESS".

Packet4: The data includes 1 "ADDRESS" and 4 "DATA".

Packet Length:

When judging the start of IIC, it is the Packet TimeStamp.



Fig4-73 - Packet Length

Packet Length: From START (Start's TimeStamp) to STOP (Unknown\_End Flag TimeStamp)

Packet Idling Length: From Unknow\_End Flag TimeStamp to Start's TimeStamp

This Unknow register is Unknow\_End Flag.



### 4.5.3 UART Analysis

### **UART Introduction**

The UART, which stands for Universal Asynchronous Receiver/Transmitter, is a serial asynchronous protocol. The UART is often time-integrated into PC communication devices, and it usually equips an EEPROM (Electronic Erasable/Programmable Read Only Memory) for error checking proposes with other chips. There are two concepts about UART which must be understood before performing any further tasks.

The UART protocol will first translate a parallel data into serial data, for the UART requiring only one wire to transmit signals. The transmission starts at a triggered Low position, and there are 7 or 8 bits of data following afterwards. To halt a transmission, it requires a signal or multiple bits of logic '1'. Odd number bit transmission requires odd parity error checking, and even number bit transmission requires even number error checking. Following the parity check is another data translation from serial data to parallel data. UART also generates an extra signal to indicate receiving and transmitting conditions.

Furthermore, since UART is an asynchronous communication protocol and data transmission may not be in bytes, a complete UART signal Packet must consist of **START**, **DATA**, **PARITY**, **STOP**, **Baud**, and **TXD** segments. They are as following:

START:	When TXD is changing from <b>HIGH</b> to <b>LOW</b> voltage (1 bit).
DATA:	Users must decide the size of signal Packet segment from 4 to 8bits.
PARITY:	This performs three types of parity checks: odd parity, even parity, and none parity.
STOP:	This occurs when TXD is at high voltage. This is adjustable; this is commonly set to 1 or 2.
Baud:	This is the data transmission speed according to the initial condition of START.
TXD:	This is the transmission direction. It is MSB $\rightarrow$ LSM by default.



### 4.5.3.1 Software Basic Setup of Protocol Analyzer UART

- **Step1.** Set up RAM Size, Frequency, Trigger Level and Trigger Position as described in Section 4.1. (Tip: The Setup of the Frequency should be higher, but not too far away from the Baud Rate of the test board).
- **Step2.** Set up Either Edge as the trigger condition on the signals which are connected to the Tx pin or the Rx pin of the tested UART board.
- **Step3.** Set up the Protocol Analyzer UART dialog box. The Protocol Analyzer UART dialog box is set as the steps of IIC.

PROTOCOL ANALYZER UART SET	UP:Bus1			×		
Configuration Packet Register	1					
Pin Assignment Protocol Analyzer Name: Bus1 Channel: A0	Protocol Analy: START	zer Color DATA	PARITY	STOP		
Protocol Analyzer Property Parity: none parity Baud Rate: 9600	Data Bit: 8 Stop Bit: 1	▼ Data D	irection: MS Rate: 70%	B->LSB 🔽		
(Min:1bps,Max:10Mbps;Users can vary the baud rate and set up the value as your requirements.) Use the reverse data level for decoding Find the baud rate automatically based on the min. pulse width						
	OK	Cancel	Default	Help		

Fig 4-74 – UART Setup

- Step4. Protocol Analyzer UART Setup
  - 1. Set the Channel of the Transmitter Signal.

Select Pin Assignment, then choose the given Protocol Analyzer name for Bus 1. Next select the signal which is connected to the pin of Bus 1 of the tested board from the pull-down menu to analyze the data of the transmitter signal.

2. Set the Baud Rate.

Select the rate from the pull-down menu of the Baud Rate to meet the specifications of the tested UART board. Baud Rate may be set and equal to 300, 600, 1200, 2400, 4800, 9600, 19200, 38400, 57600 or 115200.

3. Set the Bits for the Data Bit.

Select the number from the pull-down menu of the Data Bit to meet the specification of the tested UART board. Data Bit may be set to 4, 5, 6, 7 or 8.

4. Set the Data Direction.

Select MSB -> LSB or LSB -> MSB from the pull-down menu of the Data Direction to meet the

specifications of the tested UART board.



Fig 4-75 – Data Waveforms MSB->LSB and LSB->MSB

5. Set the Parity

Select none parity, odd parity or even parity from the pull-down menu of Parity to meet the specifications of

the tested UART board.

6. Set the Bits for the Stop Bit.

Select the number from the pull-down menu of the Stop Bit to meet the specifications of the UART DUT. Stop Bit may be set to 1, 1.5 or 2.

7. Set "Use the reverse data level for decoding".

Click on "Use the reverse data level for decoding" to decode the received data into the negative logic which a negative voltage represents the 1 state and which a positive voltage represents the 0 state.

Busi (VART)	-	 UNKNOW	START	DATA : 10110000
A DA 💊	x			

Without using the reverse data level to decode

Busi (UART)	Ŧ	UNKNOW	START	DATA : 10000000
🖌 🖌 AC	x		הווווה	

Using the reverse data level to decode

Fig 4-76 – Without/With the Reverse Data Level for Decoding

8. "Find the baud rate automatically based on the min. pulse width"

Selecting the option can help to find the baud rate automatically based on the min. pulse width.

- 9. Set Protocol Analyzer Color Click the color of the segment as the DATA, START, STOP and PARITY to select the required color.
- Step5. Press OK to exit the dialog box of Protocol Analyzer UART Setup.
- Step6. Click Run to acquire the UART signal from the tested UART circuit. Refer to Fig 4-77.
- Tip: Click 📓 icon to view all data, and then select the waveform analysis tools to analyze the waveforms.



Fig 4-77 – Waveform Analysis



## 4.5.3.2 Protocol Analyzer UART Packet Analysis

PROTOCOL AMALTZER VAR	T SETVP:Bus1	×
Configuration Packet	Register	
Item	Color	
DATA		
V PARITY		
DESCRIBE		
	OK Cancel Default	Help

Fig4-78 - Protocol Analyzer UART Packet Setup

**DATA:** List Data field captured by Bus in the packet display.

PARITY: Display parity check in packet.

DESCRIBE: Error description to any field (format or data bit).

It is a Bus Packet List view, which includes 4 formats, which UART happens below. PARITY clews whether users start PARITY or not.

B	JUS Packet L	ist						×	
	Setting Refresh Export Synch Parameter								
1	Packet #	Name	TimeStamp	DATA	PARITY			<b>_</b>	
	1	Tx Bus(UART)	207	0XC5	ODD PARI	TΥ			
ľ	Packet #	Name	TimeStamp	DATA	PARITY	, ,			
	2	Tx Bus(UART)	1247	0X85	ODD PARI	TΥ			
	Packet #	Name	TimeStamp	DATA	PARITY		Describe		
	3	Tx Bus(UART)	2392	OX7B	ERROR-1		Parity Error,should High		
	Packet #	Name	TimeStamp	DATA	PARITY		Describe		
	4	Tx Bus(UART)	3536	0XB6	ERROR-0		Parity Error, should Low	-	



Packet1: It is commonly normal Data, which includes 1 DATA and 1 PARITY; its parity is ODD PARITY.

Packet2: It is commonly normal data, which includes 1 DATA and 1 PARITY; its parity is ODD PARITY.

Packet3: It is the state of PARITY ERROR; the Describe is "Parity Error, should High ".

Certainly, EVEN and ODD are impossible to present to the same Bus. It is used for exhibition here. So EVEN and ODD appear at the same time.

Packet4: It is the state of PARTIY ERROR; the Describe is "Parity Error, should Low"

Packet Length: When judging to the start of UART, it is the packet TimeStamp.

#### State 1: Having Stop:





Fig4-80 - Packet Length





Fig4-81 - Packet Length

If the STOP falls short of condition, it isn't noted down in UART.

Packet Length: From START (Start's TimeStamp) to STOP (Unknow\_End Flag TimeStamp)

Packet Idling Length: Unknow\_ End Flag TimeStamp to START TimeStamp.



## 4.5.4 SPI Analysis

### **SPI Introduction**

SPI (Synchronous Peripheral Interface) is a parallel synchronous full duplex protocol with a Bus-like physical interface. This protocol was first developed by Motorola and was generally used for EEPROM, ADC, FRAM, and display device drivers which are equipped with low data transmission speed. The SPI data transmission is synchronous in both receiving and transmitting directions. Although Motorola initially did not define the clocking impulse, it is commonly seen that the clocking impulse is according to the master processor. In practice, there are two clocking impulses: CPOL (Clock Polarity) and CPHA (Clock Phase). The configuration of both CPOL and CPHA decides the sampling rate. When the SPI must transmit serial data, it initiates the highest bit.

Since SPI is a synchronous communication protocol and data transmission may not be in bytes, a complete SPI signal Packet must consist of SCK, MOSI, MISO, and SS segments with CPHA and CPOL. They are as following.

- SCK: Serial Clock Line (SCL).
- MOSI: Master data output, Slave data input (MOSI stands for Master-Out-Slave-In)
- MISO: Master data input, Slave data output (MISO stands for Master-In-Slave-Out)
- SS: SS stands for Signal Selector of the master device which is to select signals for the Slave devices.
- CPHA: the clock phase (CPHA) control bit selects one of the two fundamentally different transfer formats.

CPOL: the clock polarity is specified by the CPOL control bit, which selects an active high or active low clock.

the data are down and soughed	The data are driven and sampled
	JOJOJO
Clock Polarity = 0 where rising edges happen Clock Phase = 0 where wave cycle start	Clock Polarity = 0 where rising edges happen Clock Phase = 1 where wave cycle end
The data are driven and sampled	Rive dictor agree delivery angul samualerd
Clock Polarity = 1 where rising edges happen Clock Phase = 0 where wave cycle start	Clock Polarity = 1 where rising edges happen Clock Phase =1 where wave cycle end
Fig 4-82 – Clock Pola	arity and Clock Phases



### 4.5.4.1 Software Basic Setup of Protocol Analyzer SPI

- Step1. Set up RAM Size, Frequency, Trigger Level and Trigger Position as described in Section 4.1.
- **Step2.** Set up the Falling Edge on the signal of SS which connected to the Signal Selector (SS) pin of the SPI tested board.
- Step3. Set up the Protocol Analyzer SPI dialog box, the Protocol Analyzer SPI dialog box is set as the steps of IIC.

PROTOCOL ANALYZER SPI SETUP:Bus1	<u>×</u>
Configuration Packet Register	
Protocol Analyzer Setting Protocol Analyzer Name: Bus1 Mode: CPHA = 0, CPOL = 0 Follow: MSB->LSB	Pin Assignment Data: A2 SCK: A0 Custom Setting
Protocol Analyzer Color:	Custom Setting
SS Pin Assignment Activate SS Channel: A1	
ОК	Cancel Default Help

Fig 4-83 – Protocol Analyzer SPI Setup

- Step4. SPI Setup
  - 1. Protocol Analyzer Setting

Select the Mode from pull-down menu of "Bus 1".

Then Select MSB -> LSB or LSB -> MSB from the pull-down menu of the Follow to meet the specifications of the tested SPI circuit.

Then click the **\_\_\_\_\_** to set the Protocol Analyzer Color.

- **Tip:** Select MSB -> LSB to arrange data from left to right eg. 0-0-0-1=0001; select LSB -> MSB to arrange data from right to left, eg. 1-0-0-0=0001.
  - 2. Pin Assignment Setting

Select channels to set the Data and SCK channel.

Choose one channel from the pull-down menu of the Data to set the data channel.

Then choose one channel from the pull-down menu of SCK to set the SCK channel.

3. SS Pin Assignment

Click "Activate" on SS (Signal Selector).

Then select the signal which connects to the Signal Selector pin of the SPI DUT from the pull-down menu of "SS".

#### 4. Custom Setting

A. SS Setting is Activated

Click the **Custom Setting**, then the dialog box of the SPI Custom Setting will appear as shown in Fig 4-84.

- (1) Select "High" or "Low" to define the SS enable level of the tested SPI circuit.
- (2) Then type a number in Bit of the Data for the Bus signal.
- (3)Press "OK" to confirm the setup of SPI Custom Setting and return to the dialog box of the SPI Setting. (**Tip:** Press "Default" to give up the current setup)



PROTOCOL ANALYZER SPI SETUP:Bus1	×
Configuration Packet Register	
Protocol Analyzer Setting       Protocol Analyzer Name:       Bus1       Mode:       CPHA = 0, CPDL = 0       Follow:       MSB->LSB       Protocol Analyzer Color:	
S SPI Custom Setting Select Device Level Outa Outa Data Outa Bit: 8	1
✓ Iow         ✓ Virtual S5 Condition         Idling Time:       5         Us       ☑ Don't care data bit         Min : 5us       Max : 327,675ms         Default	

Fig 4-84– SPI Custom Setting

B. SS Setting is not Activated

Click the **Custom Setting**, then the dialog box of the SPI Custom Setting will appear as shown in Fig 4-85.

PROTOCOL ANALYZER SPI SETUP:Bus1	x
Configuration Packet Register	
Protocol Analyzer Setting Protocol Analyzer Name: Bus1 Mode: CPHA = 0 , CPOL = 0 Y Follow: MSB->LSB Y	Pin Assignment Data: A2 SCK: A0
Protocol Analyzer Color:	Custom Setting
Select Device Level	Dətə Bit: 3
Virtual S5 Condition Idling Time: 5 us Min : 5us Max	Don't care data bit : 327.675ms

Fig 4-85 – Virtual SS Condition Setting

(4) Type the idling time of the SCK signal on the tested SPI circuit. The idling time is defined as the idling time as shown in Fig 4-86.



Fig 4-86 – Idling Time

(5)Click on the "Don't care data bit" function. The system will restart and count from the beginning of the data bits when the condition of the idling time setting is qualified.



孕龍科技股份有限公司 Zeroplus Technology Co., Ltd.

- (6)Click off the "Don't care data bit" function, the system will decode the data stream until the bits of the data are received completely, when the condition of the idling time setting is qualified.
- (7)Press "OK" to confirm the setup of SPI Custom Setting and return to the dialog box of the SPI Setting. (**Tip:** Press "Default" to reset the current setup)
- Step5. Click OK to exit the dialog box of Protocol Analyzer SPI Setup.
- Step6. Click Run to acquire the SPI signal from the tested SPI circuit. Refer to the Fig 4-87.
- Tip: Click 📓 icon to view all the data, and then select the waveform analysis tools to analyze the waveforms.



Fig 4-87 – SPI Signal



ROTOCOL AMALTZER	SPI SETUP:Bus1	×
Configuration Pa	cket Register	
Item	Color	
🔽 DATA		
	OK Cancel I	)efault   Help

### 4.5.4.2 Protocol Analyzer SPI Packet Analysis

Fig4-88 - Protocol Analyzer SPI Packet Setup

**DATA:** List Data field captured by Bus in the packet display.

#### BUS Packet List:

S Packet	List	Contract of the local division of the	and the second se	a provide the second
etting	Refresh Expo	rt Synch Pa	remeter	
Packet #	Name	TimeStamp	DATA	
1	MOSI(SPI)	-2605093	0XD0	
Packet Ø	Name	TimeStamp	DATA	
2	MOSI(SPI)	-313945	0XD1	
Packet #	Name	TimeStamp	DATA	
З	MOSI(SPI)	1977163	OXD2	
Packet #	Name	TimeStamp	DATA	
4	MOSI(SPI)	4266271	CXD3	
Packet #	Name	TimeStamp	DATA	
5	MOSI(SPI)	6559419	0XD4	
Packet #	Name	TimeStamp	DATA	
6	MOSI(SPI)	8950527	0XD6	

Fig4-89 - Protocol Analyzer SPI Packet List

Packet Length and Packet Idling Length

1. SS channel is activated



Fig4-90 - Packet Length

Packet Length: From Unknow\_Start\_Flag TimeStamp to Unknow\_ End Flag TimeStamp Packet Idling Length: From Unknow\_End Flag TimeStamp to Unknow\_Start\_Flag TimeStamp 2. SS channel is not activated.

Virtual SS is activated 1: Data needs 8-bit; the Idling Time is set as 3us.



Fig4-91 - Packet Length

Packet Length: Unknow\_Start\_Flag TimeStamp to Unknow\_ End Flag TimeStamp

Packet Idling Length: Unknow\_End Flag TimeStamp to Unknow\_Start\_Flag TimeStamp

Virtual SS is activated 2: Data needs 8-bit; the Idling Time is set as 3us. Don't care data bit is not activated.





Packet Length: From Unknow\_Start\_Flag TimeStamp to Unknow\_End Flag TimeStamp

Packet Idling Length: From Unknow\_End Flag TimeStamp to Unknow\_Start\_Flag TimeStamp

Virtual SS is activated 3: Data needs 8-bit; the Idling Time is set as 3us. Don't care data bit is activated.



Fig4-93 - Packet Length

Packet Length: From Packet's TimeStamp Data to next Packet's TimeStamp Data

Packet Idling Length : It is 0.

The End dot is Unknown.



Fig4-94 - Packet Length

Packet Length: From Packet's TimeStamp Data to next Packet's TimeStamp Data

Packet Idling Length: It is 0.



## 4.5.5 1-WIRE Analysis

# Preface

To increase the Protocol Analyzer feature in order to analyze the Protocol Analyzer 1-WIRE transmission protocol data. Using LA analysis function, the required serial data can be converted and presented in the form of Bus. Therefore, the software needs to add a dialog box so as to set up a Protocol Analyzer 1-WIRE dialog box.

## **1-WIRE Introduction**

#### 1. Brief Introduction

#### Features

1-WIRE is a non-synchronic half-duplex serial transmission, which requires only one OWIO to transmit data. The typical 1-WIRE transmission structure is illustrated in Figure 4-95. During the 1-WIRE transmission, the OWIO can be used to transmit data and supply power to all devices connected to the 1-WIRE. OWIO will link to a 4.7K Ohm Pull-High electric resistance which is linked to the power supply (3V-5.5V). The transmission speed for 1-WIRE can be divided into two types, standard and high speed. Every 1-WIRE has a unique 64-bit code for the device to recognize. Therefore, the maximum number of link devices is 1.8; almost unlimited.



Fig4-95 - Applications

#### Applications

1-WIRE is commonly applied to the EEPROM and to certain sensor interfaces.

#### 2. Protocol Analyzer Signal Specifications

Parameter	Value
Name of Protocol Analyzer	1-WIRE
Required No. of Channels	1
Signal Frequency	Not fixed, around 10K
Appropriate Sampling Rate	1MHz
Same Data Time Per Bit?	⊡Yes ∎No
Name of Syn. Signals	OWIO
Data Verification Point	30 us after the falling edge signals

#### 3. Protocol Analyzer IO Description

Name	Function
OWIO	The only I/O transmits Reset signals and data.

#### 4. Protocol Analyzer Electrical Specifications

Parameter	Min	Тур	Max	Unit	Note
High-count Voltage	2.8		5.2	V	Every IC varies according to the Pull-High voltage.
Low-count Voltage		0		V	


### **Protocol Analyzer 1-WIRE Format Description**

Two speed types of 1-WIRE: Standard: 1MHz (1us) High: 5MHz (0.2us) Four types of 1-WIRE Signals:

1. Reset:

Every communications period starts with Reset signal. Master will send a Reset Pulse so that all the Slave devices on the 1-WIRE Protocol Analyzer enter into recognition status. When one or many Slaves receive Reset Pulse, a Presence Pulse signal will be sent back from Slave, indicating receipt of the signal.

- 2. Write 0: Send a "0" bit to Slave (Write 1 time slot).
- 3. Write 1: Send a "1" bit to Slave (Write 1 time slot).
- 4. Read Data:

"Read data sequences" resembles "Write time slot." However, when Master releases BUS and reads data from Slave devices, Master creates samples from BUS status. In this way, Master can read any 0 or 1 bit from Slave devices.

Four signal types are described respectively in the following:

- 1. Reset:
  - (1) When Master starts communicating with Slave, Master first sends a low-count Reset Pulse (TX)

of <sup>*L*<sub>RSTL</sub> (Standard speed: 480us; High Speed: 48us) for a period of time.</sup>



Fig4-96 - Master TX Reset Pulse and Master RX Presence Pulse

- (2) Then, Master releases Protocol Analyzer and enters the RX mode. Through high- pull resistor,1-WIRE Protocol Analyzer is pulled back to the high status.
- (3) Then, Master detects a rising edge from the Data Line when every slave will wait for a period of time ( $t_{PDH}^{PDH}$ ) (standard speed: 15-60us; high speed: 2-6us) and send back a Presence Pulse to Master ( $t_{PDL}^{PDL}$ )(standard speed:60-240us; high speed: 8-24us).
- (4) Finally, the 1-WIRE Protocol Analyzer will be pulled back to the high status through the resistor.
- (5) Meanwhile, Master can detect any online Slave.
- (6) From Fig4-97, the low count Reset Pulse and Presence Pulse signals can be clearly seen.



Figure 2a. You can clearly see the negative going reset and the presence pulse

Fig4-97 - Reset/Presence Detect Sequence

2. Write Data:

孕龍科技股份有限公司

plus Technology Co., Ltd

- (1) To initialize Write Data, Master will convert the Data Line from the high logic to the low.
- (2) There are two types of Write time slot: Write 1 time slot and Write 0 time slot.
- (3) During a write cycle, all Write time slots must have duration of at least 60us and a recovery period of 1us.
- (4) When the I/O line goes down, Slave devices create samples from 15-60 us.
  - A. Write 0: If the sampling is low, 0 is generated as in Fig4-98:





Fig4-98 - Write-zero Time Slot

B. Write 1: If the sampling is high, 1 is generated (Note: Read 1 is of a similar waveform pattern) as in Fig4-99:

Write-one Time Slot



Fig4-99 - Wrote-one Time Slot



#### 3. Read Data:

- (1) When Slave reads data, Master will generate a Read time slot.
- (2) To initialize Read Data, Master has to convert Data line from the high logic to the low.
- (3) Data line must be kept as low as 1us.
- (4) The Output Data of Slave must be 14us at most.
- (5) To read from 15us where Read slot starts, Master must stop driving I/O.
  - Read-data Time Slot



Fig4-100 - Read-data Time Slot

- (6) When Read Time Slot ends, I/O Pin will be pulled back to the high count through the external resistor.
- (7) During a write cycle, all Write time slots must have duration of at least 60us and a recovery period of 1us.
- 4. Typical 1-WIRE Conversation model can be summarized as below:



Diagram 1 typical 1-Wire communication sequence.

Fig4-101 - A Typical 1-WIRE Conversion

- (1) Master keeps Protocol Analyzer at low signal (standard speed: 480us; high speed: 48us) as the Reset Pulse.
- (2) Then, Master releases Protocol Analyzer and locates a Presence Pulse responded by any online Slave.
- (3) The above two points are Reset Pulse and Presence Pulse, which can be put together as a Reset Sequence.
- (4) If Presence Pulse is detected, the slave location will enable Master to access Slave using the Write 0 or Write 1 Sequence.
- 5. 1-WIRE Serial Number:
  - (1) Every 1-WIRE Slave has a unique laser memory.
  - (2) The serial number is 64bits.
  - (3) The serial numbers are 8bytes in total, located in three individual, which are illustrated as below:



MSB		64 <b>-</b> bi	t 'Registration' ROM nui	LSB		
8-bit CRC			48-bit Serial Number	8-bit Family Code		
MSB	LSB	MSB		LSB	MSB	LSB

- (4) Starting from LSB, the first byte is for family code, which is used to identify product categories.
- (5) Next, the 48bits is the only address for storage.
- (6) The last byte, MSB is used to store CRC.



# 4.5.5.1 Software Basic Setup of Protocol Analyzer 1-WIRE

PROTOCOL ANALYZER 1-WIRE SETUP:B	Bus1	×
Configuration Packet Register		
Pin Assignment Protocol Analyzer Name: Bus1 Channel: Protocol Analyzer Property Connect speed	Protocol Analyzer Color RESET PRESENCE PULSE DATA	
<ul> <li>Standard(1 us)</li> <li>High(0</li> <li>Sampling position</li> <li>30</li> <li>us</li> <li>Min:1us,Max:120us</li> </ul>	0.2 us)	
	OK Cancel Default Help	

Fig4-102 - Protocol Analyzer 1-WIRE Setup

### 1. Pin Assignment:

OWIO: Because there is only one channel for a signal, there are only two setup fields. Protocol Analyzer Name: Display the name of the selected Bus.

- Channel: Preset as A0. **2. Data Direction:**
- MSB->LSB: From High to Low bits. LSB->MSB: From Low to High bits.
- 3. Connect Speed: Standard: 1us High: 0.2us
- 4. Protocol Analyzer Color: RESET PRESENCE PULSE DATA

### **User Interface Instructions**

Set up the Protocol Analyzer dialog box which is set as the steps of IIC.



Fig4-103 - Protocol Analyzer 1-WIRE Setup

### STEP 1. Select Channel

孕龍科技股份有限公司

Zeroplus Technology Co., Ltd.

1-WIRE has only one IO. Select the channel that it is to link the IO.

PROTOCOL ANALYZER 1-WIRE SETUP:Bus1	×
Configuration Packet Register	,
Protocol Analyzer Name: Bus1 Channel: A0	
Connect speed O ata Direction O High(0.2 us) O High(0.2 us)	
Sampling position 30 us Min:1us,Max:120us Data Length 8 bit (Min:1bit,Max:32bit)	
OK Cancel Default Help	

Fig4-104 - Protocol Analyzer 1-WIRE Channel Setup

STEP 2. Set Connect Speed

1-WIRE has two modes: standard and high speed. The speed setup according to the specifications of the object to be tested and the default mode is standard.



Fig4-105 - Protocol Analyzer 1-WIRE Connect Speed Setup

#### STEP 3. Set Data Direction

Set the Data Direction as either MSB -> LSB or LSB -> MSB.

孕龍科技股份有限公司

roplus Technology Co., Ltd.

PROTOCOL ANALYZER 1-WIRE SETUP:Bus1	×
Configuration Packet Register	
Pin Assignment Protocol Analyzer Name: Bus1 Channel: Protocol Analyzer Property Connect speed Standard(1 us) High(0.2 us) Sampling position 30 us Min:1us,Max:120us	Data Direction Data Direction Data Length Bate Length (Min: 1bit, Max: 32bit)
OK	Cancel Default Help

Fig4-106 - Protocol Analyzer 1-WIRE Data Direction Setup

#### STEP 4. Set Sampling Position

Users can slightly adjust the sampling position of 1-WIRE. This feature is applicable when the signal cannot be decoded. The default value is 30us.

PROTOCOL ANALYZER 1-WIRE SETUP:	lus1	×
Configuration Packet Register		
Pin Assignment Protocol Analyzer Name: Bus1 Channel: AD Protocol Analyzer Property	Protocol Analyzer Color RESET PRESENCE PULSE DATA	
Connect speed	Data Direction	
Standard(1 us) C High(0)	.2 us) • MSB->LSB • LSB->MSB	
Sampling position 30 us Min:1us,Max:120us	Data Length 8 bit (Min:1bit,Max:32bit)	
	OK Cancel Default Help	

Fig4-107 - Protocol Analyzer 1-WIRE Sampling Position Setup

## STEP 5. Set Data Length

孕龍科技股份有限公司

Zeroplus Technology Co., Ltd.

This function decides how many bits of data can be combined as one set of figures. The default is 8 bits, and the maximum is 32bits.

PROTOCOL ANALYZER 1-WIRE SETUP:Bust	×
Configuration Packet Register	
Pin Assignment Protocol Analyzer Name: Bus1 Channel: A0 Protocol Analyzer Property Connect speed © Standard(1 us) © High(0.2 u Sampling position 30 us Min:1us,Max:120us	rotocol Analyzer Color RESET PRESENCE PULSE DATA Data Direction MSB->LSB C LSB->MSB Data Length 8 bit (Min:1bit,Max:32bit)
0	K Cancel Default Help

Fig4-108 - Protocol Analyzer 1-WIRE Data Length Setup



# 4.5.5.2 Protocol Analyzer 1-WIRE Packet Analysis

PROTOCOL AMALTZE	R 1-WIRE SETUP:Bus1			X
Configuration Pa	cket Register			
Item	Color			
🔽 DATA				
DESCRIBE	••••			
	OK	Cancel	Default	Help

Fig4-109 - Protocol Analyzer 1-WIRE Packet Setup

That is the new View; the below View includes several formats that 1-WIRE can happen; it describes Data number and their positions.

BUS Packet List							
	Setting Refresh Export Synch Parameter						
	Packet #	Name	TimeStamp	DATA			
	1	Bus1(1-WIRE)	760	OXD9			
	Packet #	Name	TimeStamp	DATA			
	2	Bus1(1-WIRE)	6210	OXD9			
	Packet #	Name	TimeStamp	DATA			
	З	Bus1(1-WIRE)	11660	OXD9			

Fig4-110 - Protocol Analyzer 1-WIRE Packet List

Packet 1: It is commonly normal DATA, which includes 1 DATA.Packet 2: It is commonly normal DATA, which includes 1 DATA.Packet 3: It is commonly normal DATA, which includes 1 DATA.Packet and Idling Length: Packet's TimeStamp is Reset.



### 4.5.6 HDQ Analysis

### Preface

Increase the Protocol Analyzer feature to analyze the Protocol Analyzer HDQ transmission protocol data. Using LA analysis function, the required serial data can be converted and presented in the form of Protocol Analyzer. Therefore, the software needs to add a dialog box so as to set up a Protocol Analyzer HDQ dialog box.

## 4.5.6.1 Software Basic Setup of Protocol Analyzer HDQ

### **HDQ Introduction**

#### 1. Brief Introduction

#### Features

Protocol Analyzer HDQ is a non-synchronic half-duplex serial transmission, which requires only one HDQ and uses a quasi-PWM (Pulse Width Modulation) to verify the serial data.

#### Applications

HDQ is commonly applied to the display interface for battery management.

#### 2. Protocol Analyzer Signal Specifications

Parameter	Value				
Name of Protocol Analyzer	HDQ				
Required No. of Channels	1				
Signal Frequency	Not fixed, around 12MHz, 13MHz and 19,2MHz				
Appropriate Sampling Rate	100MHz				
Same Data Time Per Bit?	□Yes ■No				
Name of Syn. Signals	HDQ				
Data Verification Point	Low signals > 190us converts to High signals > 40us				

3. Protocol Analyzer IO Description

Name	Function
HDQ	The sole I/O transmits Host and BQ-HDQ status and data.

#### 4. Protocol Analyzer Electrical Specifications

Parameter	Min	Туре	Мах	Unit	Note
Logic Input High	2.5			V	
Logic Input Low			0.5	V	

## **Protocol Analyzer HDQ Format Description**

The format changes according to the pulse width, so the display must refer to the defined pulse width. Protocol Analyzer HDQ is made up of 16 bits signals. Firstly, after the period of status signals, a device will be installed for the 7 bits address through the Host so that 1-bit signals can be read or written. After a response time of high signals, data will be exported in 8 bits format with the data and location content from LSB to MSB. The following is the Host to BQ-HDQ analysis.





Fig4-111 - Host to BQ-HDQ Analysis

## **Protocol Analyzer Format**

#### Break

This is the initial bit for the Protocol Analyzer HDQ: after Low signal lasting a period of t (B), it is then converted to a High signal lasting a period of t(BR). The length of Low signal is no less than 190us whereas the High signal is no less than 40us.



Fig4-112 - Pulse from Low to High

#### Address

The Address comprises 7 bits. The initial Low signal lasts a period of t(HW1) and if the write-0 status continues through the end of the t(HW0) period, the signal will convert to High and last throughout the period of t(CYCH), as shown by the dotted line in the following figure. Conversely, if it is the write-1 status, after t(HW1) period of time, the signal will convert to High and last throughout the period of t(CYCH), which is of 1 bit and no less than 190 us. The t(HW1) range is from 0.5us to 17us and no more than 50us. The t(HW0) range is from 86us to 100us and no more than 145us.

### Read/Write

Read/Write is 1 bit. 0 and 1 are displayed in the same way as the above description.

#### T (RSPS)

The High signal lasts a period of 190us-320us. The following 8-bit data is Send Host to BQ-HDQ or Receive from BQ-HDQ Data.

#### Data

Made up by 8 bits, and it is Send Host to BQ-HDQ or Receive from BQ-HDQ Data. It operates in the same way as in 2.2 and the data is from LSB to MSB.

#### **BQ-HDQ To Host**

If the data transmission is read by BQ-HDQ To Host, the initial Low signal lasts a period of t(DW1) and if the write-0 status continues through to the end of the t(DW1) period, the signal will convert to high and last throughout the period of t(CYCD), as shown by the dotted line in the following figure. Conversely, if it is the write-1 status, after t(DW1) period of time, the signal will rise and last throughout the period of t(CYCD), which is of 1 bit and ranges



from 190us to 260us. The t(DW1) ranges from 32us to 50us and no more than 50us. The t(DW0) ranges from 80us to 145us.



Fig4-113 - Signal from BQ-HDQ to Host

## User Interface

Set up Dialog Box Description

PRO	TOCOL ANALY2	ER HDQ S	ETUP	Bus1					×		
C	Configuration Packet Register										
	Pin Assignment Protocol Analyzer Name: Busi Channel: AO										
	-Timing(VS) -								-		
	Break:	190	to:	1000000	Recovery:	40	to:	1000000			
	Host 1:	0	to:	70	Device 1:	0	to:	70			
	Host O:	80	to:	180	Device O:	80	to:	180			
	Host bit:	190	to:	260	Device bit:	190	to:	260			
	🔽 Response:	190	to:	320							
	-Protocol Ana	lyzer Colo	r —								
	BREAK	RECOVED	RΥ .	ADDRESS	READ	WRITE		DATA			
			[	OK	Cancel	Defa	ult	Help			

Fig4-114 - Protocol Analyzer HDQ Setup

### 1. Pin Assignment:

HDQ has only one signal channel, therefore it only specifies the name of the channel and marks the selected channel.

Protocol Analyzer Name: Display the name of the selected Bus.

Channel: Preset as A0.

### 2. Timing:

Set the time for BREAK, ADDRESS, READ/WRITE, DATA and RECOVERY.

### 3. Protocol Analyzer Color:

BREAK

RECOVERY

ADDRESS

- READ
- WRITE
- DATA



## **Operating Instructions**

Open the LAP operation interface.



Fig4-115 - Operation Interface

Sample the HDQ signal or open the sampled waveform.

() () () () () () () () () () () () () (	8 11	A Si C C III	- 2 0.0061	0.35! - 😵 📰	80 12 12 12 1 C	M 10 01 100	Eright	26 • Trigger Dels k - 8 = 30 • Comprodute 118.280
tm/Signal	Tricer	Filter D	-107648 -104	eres -163964	-1(1920	<b>P</b>	528	245754 527624
× 10 10	1.	0.		and the second second	and			
1 M AL	UL I	- 10 F				No.		
120	8	- 60						
× 10 10	10	0						
# M. M.	HI I	10						
18.11	18							
F 10	1日	0				-		
# AT.141	36	10						
1 10	12	10						
/ 31	15	0						
12	10	8						
10	R.	0.00						
<b>3</b> 34 11	18	0						
15=	III	10						
18	8	0						
10.00	10.0	0						
1000	8	0						
/ Ci @	101							
102	8	0						
	and the second s	A DECISION OF THE OWNER.						

Fig4-116 - HDQ Waveform



Arrange the signal channels into Bus.

+ 16394 1 10025881		Staplar Tripper	Era II Era II	A Pog -128402 D Pog -128408		- T = 138408 +	k - 8 = 30 + Corpe=Sale 136 283
a/Sigial	Trigger	Piller 1	421EBO	-045760 -160040	-10 KK 1-		69049 <u>24575</u> 8 <u>8290</u> 24
€ Zy Charas	ds Sotup		-		-		
And the first	Tatalan,		-				
Or Ha	into Sur	Our19	-9				
-	and .		211				
· Capy C	hansl						
Dulots	All Chants	la .	-				
Basto	· Defects C	hands					
· Scours	10		10				
0 13 D	×	-00					
× 84 11	10	8					
<b>2</b> 85 m	10	8					
¥ 88 H	26	6					
# 27 TT	- 25	- 15					
100 10		15					
<pre>/n</pre>	11	- 11					
4.12	28	181					
		a second s					

Fig4-117 - Group into Bus

Select Bus Property.

Septing Strip     Septing	Le 18384		Binglap Fee Tripper Fee	0	A Pag -1396418 + 8 Pag -1396418 +	A - T = 1794418 + 8 - T = 1794400 -	A - 3 = 30 + Centrefate 133 285
Serging Stop     Sorging Stop     S	ha/Sigial	Trigger	Filter D	-821536 -2455	co -ucosta -store	w1420 1654	40 245300 027880
Comparison Servery     Comparison Server	Lane .		Total Party	I I I I I I I I I I I I I I I I I I I		X IN XXXXXXXXX	* * a YYIIa Y
Image: Second	N O	amala Serap	1				
Image: Section of the section of t	× 11 11	n Bripsrif ,					
Notes     Curity	12	allow Yeroftan					
Image: Second	× 01	erer beste finne	CH10				
Image: Section of the section of t	# A3	group cros p	ar curre	-			
Interferment         Interferment           Filter Marsh         Interferment           Interferment         Interferment	15	er Diereil		25			
State AL: Assessive         State AL: Assessive           Batters: Infant: Datasite	F # 1	Cele (Carale)					
* 80         * 100           * 80         * 80           * 80         * 80           * 80         * 80           * 80         * 80           * 80         * 80           * 80         * 80           * 80         * 80           * 80         * 80           * 80         * 80           * 80         * 80           * 80         * 80           * 80         * 80           * 80         * 80           * 80         * 80	1.17 1.	lata All Cha store Referi	mela 1 Characta				
Image         Image           Image <td>/ HO T.</td> <td>ense Rea</td> <td></td> <td></td> <td></td> <td></td> <td></td>	/ HO T.	ense Rea					
	· 11 3.	E 101-1		5.00			
	1 H K	8	- 61				
	00 11	100	8				
M         G           100         10           101         10           102         10	× 19 11		0				
	<b>/</b> 15 =	10	6				
X         B           /mm         X         B           /mm         X         B           /mm         X         B	18						
	1 27 11	18	8				
	1.00		-8				
	< n n	16	8				
			Street and st				

Fig4-118 - Bus Property



Select the decoding function of the protocol analyzer HDQ and select OK to confirm.

🕑 🖬 🔳		N N P B P P	A Test -CENTRY -	A - T = 138408 m	ht 26 * Trigger Delay
A 18025081		Trigger Fex.0	D 7va =1394000 ( +	a = 1 = 1394300   +	Corportinate 538-283
Suc/Signal	Trigger	Polton -spitab	-145360 -163048 -91820	41 0EB 16300	IN DESTEN RENDER
(100 (i)	1	Bas Property	×	TWINNIN W	XXXXLXLXLL
- 10 ×	1	General Bux Setting	1		
/ AL 11		C Gerwend Dasc	- Tractority		Take Nutristication
18.		E Advartessionen	AL (*		
(A) (A)	50		Next Analysis		
# ## III	18	Protocol Analyzer Setting			
16 -	30	G Detect Anders	Parameters config		
10	32	PROVIDE NOT OTHER			
100	36	C ZEROPLUS LA EIC NODULE	10.1/		
¥ 10	16	C 20ROPLUS LA SP12.0 MOD C 20ROPLUS LA SP12.0 MOD	AE V1.02 AE V1.02		
1 H H	36	C 28ROPULS LA 120 EEPROP	24033 MODULE V1.00		
/ 12 =	55	C 2010PUUS LA PHORE PRO	OF ALM		
(0 15	38				
. In 14	510	1 200000000000000			
1 10 10	36	P use the bubs	me l		
1.00	R	More Photocol Analyzen 162x	University of the loss of the		
FET	32	0	Cance Hep		
/ 00	H	10			
100	18	8			
10	56	18			
ALCONE.					

Fig4-119 - Protocol Analyzer HDQ Setup

Complete the protocol analyzer HDQ decoding.

ral.e 16394		k St ()	Pen Zar	12 B.D	1610351 A b	- 12 E		12	A - 1 = 3 - 1 -	134418	** Beiel	H 26	- 8 = 10 - 8 = 10	- 138.289	Dalay
Ma/Stg.d	Trigger	Tilter	L. A	- per .	19410,857	194222	ant parts	₹ <b>7</b> 65 \$	196 31100	414992.0	17 490512	.287 . 17	49.90 29.7	<b>1</b> 96492	क्ष्म एव
Ev. (994)	1	10 ·										DATA			n n
V AL	1R	8	-				u u u	1				ц н			
112	12	8													
(AL 47	10	8													
· **	10	8													
18	10	10													
10	10	8													
1.17 -	24	18													
/ 10 10		8													
# M H	36	8													
/ 12 11	100	8													
68.10	10	0													
# 14 IN	10	18													
1 88 -	18	8													
18		「「「「」													
4 BT 11		8													
100		8													
		R. C.													
× tt =	125	and the second se													

Fig4-120 - Protocol Analyzer HDQ Decoding



PROTOCOL	. AWALYZER HD(	Q SETUP:Bus1			×
Configu	ration Packet	Register			
I	tem	Color	Item	Color	
V	BREAK		VRITE	• • •	
	RECOVERY		JESCRIBE	••••	
V	ADDRESS	• • •			
V	DATA	••••			
V	· READ				
			1	1	-
		OK	Cancel	Default Help	

# 4.5.6.2 Protocol Analyzer HDQ Packet Analysis

Fig4-121 - Protocol Analyzer HDQ Packet Setup

**Item:** Select the content which needs to display in the Packet List, which includes BREAK, RECOVERY, ADDRESS, DATA, READ, WRITE and DESCRIBE.

Color: Set color for items which needs to display in the packet list.



### 4.5.7 CAN 2.0B Analysis

### Preface

Add Protocol Analyzer function to analyze CAN 2.0B transport protocols data. CAN 2.0B serial transmission, there are two signal channels, CANH and CANL, which match with baud ratio judge serial data. If you want to change serial data into Bus format, you need to analyze this function with LA. a dialog box needs to be added; you should set up a Protocol Analyzer CAN 2.0B dialog box.

## 4.5.7.1 Software Basic Setup of Protocol Analyzer CAN 2.0B

### **CAN 2.0B Introduction**

#### 1. Brief Introduction

#### Features

CAN 2.0B (Controller Area Network) is an Asynchronous Transmission Protocol. It costs low, sky-high use rate, far data transmission distance (10KM), very high data transmission bit (1M bit/s), sending information without appointed devices according to message frame, dependable error disposal and detection error rule, message automatism renewal after damage, and node can exit Bus function on the serious error.

#### Applications

CAN 2.0B is used for automotive electronics correlation systems connection.

#### 2. Protocol Analyzer Signal Specifications

Parameter	Value
Name of Protocol Analyzer	CAN 2.0B
Required No. of Channels	1
Signal Frequency	Not fixed, around 12MHz, 13MHz and 19,2MHz
Appropriate Sampling Rate	100MHz
Same Data Time Per Bit?	⊡Yes ∎No
Name of Syn. Signals	CAN 2.0B
Data Varification Boint	Low signals > 190us converts to High signals >
	40us

#### 3. Protocol Analyzer IO Description

Name	Function
CANL	The main signal source of transmission data
CANH	Signal is opposite to the signal source of transmission data

#### 4. Protocol Analyzer Electrical Specifications

Parameter	Min	Туре	Max	Unit	Note
Logic Input High	2.5			V	
Logic Input Low			0.5	V	

## **CAN 2.0B Frame Specification**

CAN 2.0B can separate into frames as follows: Data Frame, Remote Transmit Request Frame, Error Frame, Overload Frame. Because CAN2.0B is transmitted by the format of different signals, the signal can separate into CANL and CANH, and the signal direction of CANH is opposite to that of CANL. Next we analyze CAN 2.0B signal



with the standard of CANL.

### **Basic Data Frame**

Data frame can be divided into Basic CAN and Peli CAN, Data Frame of Basic CAN transmission. As follows, message data can be separated into Start of Frame (SOB), Arbitration Field, Control Field, Data Field, CRC Field, Ack Field, End of Frame.



Fig4-122 - Basic Data Frame

### **Start of Frame**

Every Start of Frame must be 0, which means asking far data to come back.

### **Arbitration Field**

Identifier is 11bits; its function is the sequence when transmitting signal, numerical value is lower, the priority is higher, and the array is from ID-10 to ID-0, and the numerical value is not all from ID-10 to ID-4, finally RTR(Remote Transmit Request) is the judgment bit of transmission or Remote Transmit Request. When RTR=0, it denotes that the data goes out; when RTR=1, it means asking far data to come back.

## **Control Field**

Control Field consists of 6 bytes, including Data Length Code and two Reserved Bits as Peli frame for future expansion. The transmission reserved bit must be 0. Receiver receives all bits combining 1 with 0. As the below figure, IDE and RB0 of Control Field are Reserved Bits which must be 0 and the latter 4bits are only 0-8 which denotes the data behind will transmit several bytes data.



Fig4-123 - Control Field

## **Data Field**

The Data Field consists of the data to be transferred within a Data Frame. It can contain from 0 to 8 bytes, and



each contains 8 bits which are transferred MSB first.

# **CRC** Field

16bits CRC, the last is a delimiter, and the default is 1.



Fig4-124 - CRC Field

### Ack Field

That is the return signal of Receiver, which has 2 bits, and the final is a delimiter whose default is 1. If receiving success, Ack will send back 0, then the transmitter knows the Receiver has received the data.

## **End of Frame**

1111111 denotes end.

### Peli Data Frame

In the Peli Data frame, Data Frame as follows, the frame of message is separated into Start of Frame (SOB), Arbitration Field, Control Field, Data Field, CRC Field, Ack Field, End of Frame. However, the parts of Arbitration Field have much more than 18bits and the SRR and IDE are 1.



Fig4-125 - Peli Data Frame

# **Remote Transmit Request Frame**

When RTR=1, it denotes Remote Transmit Request Frame, at this time, DLC3...DLC0 are the Data bytes of

return data. And the frame doesn't have Data Field.



Fig4-125 - Remote Transmit Request Frame

## **Error Frame**

The Active Error Flag consists of six consecutive Data Field 'dominant' bits. Dominant bits violate the law of bit stuffing. All bits can produce Error Frame after recognizing bit stuffing wrong, the Error Frame called Error. Corresponding Error Flag Field includes sequence bits from 6 to 12 (which produces by 1 or more nodes). Error Frame ends in Error Delimiter field. After Error Flag sends out Bus actively to get the right state, and the interrupted node tries its best to send abeyant message Error Delimiter. Error Delimiter consists of eight 'recessive' bits and allows Bus node to restart Bus transmission after Error happens.



Fig4-127 - Error Frame

## **Overload Frame**

There are two kinds of Overload conditions, which both lead to the transmission of an Overload Flag. The internal conditions of a node which require a delay of the next Data Frame start during the first bit of Intermission. Overload Flag can send six '0', which may damage Intermission format so that it makes the other nodes know node sending Overload Flag at this time. When Overload Flag is sent out, Overload Delimiter can send eight '1', others send seven '1'after finishing either.



Fig4-128 - Overload Frame

## **Interframe Space**

Interframe Space is divided into Intermission and Bus Idle. Intermission is three '1'. It is impossible to send any message during this time, except Overload Frame. The Bus is recognized to be free; the period of BUS IDLE may be of arbitrary length. And any station having something to transmit can access the Bus. When a node is at the state of 'error passive', the node will send eight '0' after INTERMISSION and other node have the chance to retransmit themselves information.

## **User Interface**

PROTOCO	IL ANALYZER	CAN 2.0B SETUP:	:Bus1		×
Configu	ation Packet	Register			
⊢ Pin A	.ssignment			Data start	
Pro	tocol Analyzer	Name: Bus1		@ 1116	totart
Che	annel: 🛛	10 <b>•</b>			( stan
	Use the revers	e data level for deco	oding	O bit :	start
- Proto	icol Analyzer Pi	roperty-			
Bau	id Rate: 1	25000 💌	Perce	ntage sample: 60	% 🔽
(Mir and	n:1bps,Max:10M set up the valu	Abps;Users can vary ue as your requireme	y the baud rate ents.)		
	After "End of F	rame'' happens,just	begin to analyze		
	When CAN Da	ita for expansion, co	ombined Basic ID a	nd ID	
	Auto-Judge Ba	ud Rate (suggest ad	dopting high sampli	ng rate to carry on da	ta sampling)
Proto	icol Analyzer Ci	olor			
9	TART	CONTROL	CRC	ERROR	ACK
	END	ID	DATA	OVERLOAD	NACK
			OK Ca	ancel Defaul	t Help

Fig4-129 - Protocol Analyzer CAN2.0B Setup

**Pin Assignment:** CAN 2.0B signal can be divided into CANL and CANH, and the default is CANL. **Use the reverse data level for decoding:** Reverse the data.

Data Start : It can be divide into two forms, 111 bit start and 0 bit start.

### **Protocol Analyzer Property**

**Baud Rate:** Input the baud rate by hand directly, and the baud rate is an integer. the default is 125000; the list includes 5, 10, 20, 40, 50, 80, 100, 125, 200, 250, 400, 500, 666, 800, 1000, 2000, 125000..., and the biggest one is

10M. Users can vary the baud rate and set the value as their requirements.

**Percentage Sampling:** Input the position of the sampling dot in baud rate; the default is 60%; the range is 25%~75%. And the default can be adjusted by 1; the list is one option of interval 5%. If the below is selected, the decoding function can work after the end of the frame. Combination extends format: Progress Basic ID and ID Protocol Analyzer Color: START, CONTROL, CRC, ERROR, END, ID, DATA, OVERLOAD, ACK and NACK.

### **Operating Instructions**

Turn on the user interface of the Logic Analyzer.



Fig4-130 - User Interface

ALC: NO	Git (21.	1 100 10	TTT & AM	mill as I	1206 1	Tel and Tel	URANI-	1	- MAN	100	1 44	10		1	-
	1 000 144	N 163 100	AL P PP	100 0244	1286 - 1		D To +	-	at 190	-1-41 41	Bataba	200	100	in the second	-
and a . 42%		4 Bi Ci	y Jon 199771	10.0244	A Pear	83467 -	Er for fa		T = 6040		the Lot	4-1	7 30	+	(e130)
stal 39900722		Trizpe	r Post.0		B Post	50437 ×		1	T = 6043	T 💌		Conpr	Sate :	128, 179	
ha/Sigel	Tripper	Tilter	16637.	967	8.067	697.067	20097.067	50171.	6T	51,167	104507.06	7	067	589492	06T 280
100	1.														
- A1 1	R	8				-					(179) 	-			-
120	-16	8													
( kg 10	R	1.65													
- # M +	381	8													
1.6 1	32	- 22													
116 -		8	-												
241	50	0													
/ 10	- 10	003													
<b># 31</b> 11		10													
181	22	10	-												
(10 II)	20	18													
* 16 (16		8													
15 1	18	10													
180	10	0													
1 IT II	00	8													
1000	25	8													
e ci 🗉	16	0													
1000	10	() (注)	-												
000	181	8													
. 04	11	8													

Sample the CAN 2.0B signal or open the sampled waveform.

Fig4-131 - CAN 2.0B Waveform



Group the signal channels into Bus.

DESCRIPTION LAP-O	(322960) (	5/1 - 000000 Bra/Stan	Bata Tools Y	diell			
	2 2	and gring	TTO N N	1 1 1 2 1 2 1 2 1 1 1 1 1 1 1 1 1 1 1 1		de Pass 1 w	Court 1 x
	-	h H	100 100	The stand all a fill and the Re	To a state of The	Buists DE	al Taining Tained
50 50 858 158 Seals 4006		N Ni C	Art. Page 190577	A Tos -80487 -	A- T - 64951	- A-	- licittat seral i
f=tal 16600722		Trias	per Pas II	5 Fox:-58437 -	3 - T = 68407	· Corp	e-8ats:108.179
Bur/Signal	Trigger	Falser 1		NOT 071-07, 067 57617, 067 700	AT. NGT - SHETT. NG7 - 11 8087	OFT EPOTET NOT 16481	17.067 148447 067 2807
	10				AD CANCEL SALE AND AD CANCEL PROPERTY ADDRESS ADDR	server serve or ner of server o	
1 1 Saug	pling Setup						
it, the	mals Setter						
	In families						
-	an inte Des		C1/116				
- Orr	trei frie fe	2	CHES ALL				
	Dureal						
d'A Cop	Chasel						
- #A Dala	ets Channell						
- /3 DeL	ets ALL Char	atla					
- /3 Bast	tore Jafanlt	Chanals					
/1 For	bat Bre						
	1 20 1	0.0					
31 71	38	1					
18.8	30	10:					
- / 22 11	00	-					
- / 31 11	38	8					
100	38	- 22					
10	52						
100		-					
-	200						
13							
a ca ca	111.1	1.					
			A 4				All Break days

Fig4-132 - Group into Bus

Select the  $\ensuremath{\text{Bus Property}}$  to set up the Bus Property dialog box .

TRUPUS LAP-	(322960) (	3/1 00000	(00001) - (1	deel]						-10	×
Co phi Ip/Sipi	al Trigger	Stat. Stat	Sats Locis 3	indor Bilp		Caner -	I A PART	La e la			X
	-	1 1 1 1		12	SK - Her Int	Summe -	Tes pine .	- Page  1	· Count	1 1	-
Color Bar Les		RNC	7 III       +	0.024414	A 200 - 50487 W	E 1 2 1		Bright	26 - 10	igger Delay	-
Tutal 10000722		Trias	per Paul		8 Fog88437 -		1 - T = 68437	-	Corper Bate:	E20.179	
Pro/Signal	Triager	Piliter		AND DESCRIPTION	10. 10012 012	THEAT BAT	-	CONT LINET. M	T DATE T. M.T.		
- Beal		0	1	Y	- TY -	YTY	YY	YY	YY	YHDING	1
1	Comp 21 or b 1					1			<u> </u>		ř
1	Channels 3	leter					hand 1		-		1
A 47 - 10	Des Proper	(19)		-							-
	(4)(12.44	nije.+		-							-1
-	George Land	(Inc.	Chirs/								
	Unarona di	ron Sea	Ctr1+#								-
46 11	Ald Dates	a									-
- # AL 15	Copy Church	HS .		-							-
AT AT	DeLets ALL	L Charaolt									-
# 30 10	Beators 1	failt Class	als								4
- / 31 11	Format Rev	opolomen D									
- / 8 -	Beause										
- (22.21	38	1.12									-
	- 31	0									
- 135 11	-50	8	1								
- /8 -	.00	6									-
- 4 31 7	30	-8									
	12	10									
100	50	5									-
-/00	34	0									-
0.0	30	63									
										2	É
last 17	L'OR CHARTER	54 H	Station -						and .	Reports the no	6 2

Fig4-133 - Bus Property



Select the decoding function of the protocol analyzer CAN 2.0B and select OK to confirm.

fulle figulitional	Toluer	Leville	onini	الم الع الحال من الحال من المحمد المحمد الم
D 🕑 🔐 🗐 Seale 49% Tetal 37590238		4 1 1 1	Image: Point of the state of the s	Image         Image <t< th=""></t<>
ha/Sigad	friger	Tilter	Ins. Francistr all	451, 8,
- Dail			General But Setting	XXXXXXXX
/ XO =	I	0	C devendes cal+centra	
	111	0		
140	10	1.001	Entry frames +	
(AS 10	28	0		
M - 11	18	0	wroteca wranger backing	
115 1	31	0	Paratectil Analyzer     Paratecters Config	
14	50	0	C 2EROPULIS LA HEQ PRODULE V2.05	
# AT 10	21	07	C 25HOPLUS UA SM 2.0 PHODULE V1.72	
/ 30 11	10	8	/* 22ROPLUS LA PM L.3 PRODULE VILOR /* 22ROPLUS LA I2C(EERROM 2NUX) MODULE VILO3	
/H 11	30	0	C ZEROPLIS LA 3-WERE MODILE VI. DI	
<b>/ 10</b> 11	25	8		
	RI	18		
- 34 H	- 01	6	12 Use the Disco Prid	
181	10	0	Mane Protocol Analyzer: http://www.neroplan.com.tw	
18	38	.0	OK Cancel Help	
111	X	- 55		
1000	30	8		
10	35	1.22		
100	24	8		
000	10	0		
1.	1 1 1			and the second sec

Fig4-134 - CAN 2.0B Bus Property Setup

Double click the ZEROPLUS LA CAN 2.0B Module V1.09 to set the Protocol Analyzer CAN 2.0B Setup dialog box.

ROTOCOL ANALYZE	R CAN 2.0B SETUP	:Bus1		x
Configuration Pack	ket Register			
Pin Assignment			Data start	
Protocol Analyz	erName: Bus1		• 111bit	start
Channel:	A0 💌			
🗌 Use the reve	erse data level for dec	oding	◯ 0 bit st	art
– Protocol Analyzer	Property			
Baud Rate:	125000 💌	Percer	ntage sample: 60%	: 🔽
(Min:1bps,Max:1 and set up the v	OMbps;Users can var alue as your requirem	y the baud rate ents.)		
After "End o	f Frame'' happens,just	begin to analyze		
🔲 When CAN I	Data for expansion, co	ombined Basic ID ar	nd ID	
🗌 Auto-Judge I	Baud Rate (suggest a	dopting high sampli	ng rate to carry on data	a sampling)
- Protocol Analyzer	Color			
START	CONTROL	CRC	ERROR	ACK
			· · · ·	
END	ID	DATA	OVERLOAD	NACK
		OK Ca	ncel Default	Help

Fig4-135 - Protocol Analyzer CAN 2.0B Setup



Click OK in the Protocol Analyzer CAN2.0B Setup dialog box to complete the CAN 2.0B Setting.

	1 21 0	14 24	11 1972	NN	faces al.M.	Interior -	m 12 fun	S al de Perso	1	al dent fi	1
	IN OF	5 51 /		- K 0.015	1147 - 2 -	B. B. T. +	14	100 215 ··· 15	alakt 25	- Teire	er Deles
ale:020		Diegó	ing Test 170	25	A Pag -142782	*	A - T - 1	13182 +	A	- 1 - 30 +	es estart
+141-33395022		Trip	per Post 0		1 Pro.~147730	*	8-1-1	1373E   •	Ce	127.36 age=Bate:127.36	82
Profiliant	Trigger	TILME	2	1204.1	1904.11 105644		srout a	201066 C . 20	M206 T	28.8844.8 202	100 A 10
and (TMR 5	1		DAUS NUS	00000 1 00000		TWOM I	E M	BC 18   00014	0000	0%1 (MIR)	
<b>/ X</b> 0	ж	- 8						תתת			
# A1 11	10	0									
124	- 38										
(A) A	10	8	L								
# 35 LI	0.25	- 8									
<b>1</b> K H	8m-	0									
161	18	()									
1 KT VI	11	0									
<b># 10</b> 10	.16										
# 11 II	18	一種									
120	-28	- (8									
- 13 33	10.00	每									
# BE 01	18-	8									
15 2	10	8									
18=	1 22	8									
<b>2</b> II 11	-33	6									
100	110	- 68									
🖌 CI (1)	381	(8									
100	0.88	-									

Fig4-136 - CAN 2.0B Decoding



# 4.5.7.2 Protocol Analyzer CAN 2.0B Packet Analysis

PROTOCOL AMALYZER CA	N 2.0B SETUP:Busl	X
Configuration Packet	Register	
Item	Color	
🔽 ID		
CONTROL		
🔽 DATA		
ACK		
V NACK		
DESCRIBE		
	OK Cancel Default Help	

Fig4-137 - Protocol Analyzer CAN 2.0B Packet Setup

Packet color can be varied by users.

The Packet displays with the waveform as below:

			in	00765	12 - 1	2 24 0	. D T			as rage	ZE + Teta	per Delar
ale 33086 tal 33386827		Display For 1 Brigger For 1	121147		A Peg	143752 *			A - T + 143782 - B - T = 143732		A - 3 = 30 + Corpe-Bate 127	भव
hadigal	Tricper	71110	54517.1	12990	1. 5.1	5 19190	2646	4.9			. 541991 S . 5	
				1113	X	CORTER N	N/int		835		LUC	
1 43	x				1	הההד		nn r				10
/ x1 == -	10	8					10 1		100	1.5	122	8
120	32											
0.00	10	10										
A 84. 10	15	8										
100	52	.0										
1.		10										
		0										
	-											
/ 10	1.1.1.1	distant in										
toting   Refre	D E-port	Synch Statutes	nu l									
Subscription in the subscription of	Distant.	Trentition	and a second second									
Exclusion and		0 101120	001300	378	IN							
Fachat #	#1(CAN 2.08			and the second se			Contraction of the local division of the loc	ACT.	Date: Bat			
Packat # 1 Dr Packat #	nil(CAN 2.08	TimeStamp	BASIC ID	1.01.0		and second	20120					
Fadot # 1 Dr Fadot # 2 Dr	nii (CAN 2008 Féirne nii (CAN 2008	TendStamp ) 173652	CHID2A	RTR	IS R	an DKI	NORG	14600	ACK ERROR			
Factor # 1 Dr Pactor # 2 Dr Pactor # 3 Dr	n1(CAN 2.08 n1(CAN 2.08 n1(CAN 2.08	TimeStamp 172652 TimeStamp		RTR	TE R	aD DKL	NORC CRC	NACK ACK	ACK BRROR			
Factor # 1 Dr Fuctor # 2 Dr Factor # 8 Dr Factor #	ni (CAN 200 Natina Natina Natina Natina Natina Natina	TreeStarp) 172652 TreeStarp 662816 TreeStarp		R TR R TR	IDE R	80 DKL	NORC CORE NORC	NACK NACK	ACK ERROR Detter bei ACK ERROR			
Fachart # 1 D Packart # 2 Ba Packart # B Ba Packart # 4 Ba	HI (CAN 200 Fairtea FII (CAN 200 Fairtea Fairtea Fairtea Fairtea Fairtea	TimeStamp 172652 TimeStamp 0 662016 TimeStamp 5 5350952		RTR RTR RTR	DE R	80 DKL 80 DKL 80 DKL	NORC NORC NORC NORC	NACI: NACI:	ACK ERROR Describe ACK ERROR Describe ACK ERROR			
Fachart # 1 Dr Trachart # 2 Re Precisent # 8 Re Precisent # 6 Re Frachart #	ni (CALEA Farma Farma Farma Farma Farma Farma Farma Farma	TimeStamp 172652 TimeStamp 0 662816 TimeStamp 1390992 TimeStamp		RTR RTR RTR	DE R	80 DK1 80 DK1	NORC CRC NORC CRC NORC	NAO: NAO: NAO:	ACK EPROR ACK EPROR ACK EPROR ACK EPROR ACK EPROR Describe			
Padout # I Ba Padout # Padout # Padout # Padout # 5 Da	Tarna Farna Farna Farna Farna Farna Farna Farna Farna	TendStamp 172652 TendStamp 662816 TineStamp 5380952 TineStamp 5380952 TineStamp 5380952		RTR RTR RTR RTR	DE R DE R DE R	80 0×1 80 0×1 80 0×1	NCRC CRC NORC CRC NORC CRC NCRC	NAOK NAOK NAOK NAOK	ACK EPROR Describe ACK EPROR ACK EPROR DESCRIDE ACK EPROR			
Fadout # 1 Da Padout # 2 Da Padout # 8 Da Padout # 5 Da 6 Da	Tache Fache Fache Fache Fache Fache Fache Fach Fach Fach Fach Fach Fach Fach Fach	TendStarp) 172652 TendStarp) 662816 TeleStarp) 1330952 TendStarp) 3620796 1962517		RTR RTR RTR RTR RTR	DE R DE R DE R	80 0×1 80 0×1 80 0×1 80 0×1 80 0×1	NCRC CRC NCRC CRC NCRC CRC NCRC CRC	NACK	ACK ERROR Describe ACK ERROR Describe ACK ERROR Describe ACK ERROR Describe ACK ERROR			

Fig4-138 - CAN 2.0B Packet List Displayed with the Waveform



# 4.6 Compression

The compression function enables the system to compress the received signal and has more data stored in per channel.

### 4.6.1 Software Basic Setup of Compression

- Step1. Set up RAM Size, Frequency, Trigger Level and Trigger Position as described in Section 4.1.
- **Step2.** Set up the trigger edge on the signal or the Bus to be triggered.
- Step3. Click 🔟 icon, or click the compression function from the Sampling Setup dialog box then click Apply and OK to run.

US LAP-C (16128) (S/	N:000000001) - [LaDoc1]
B <u>u</u> s/Signal T <u>r</u> igger	Run/ <u>S</u> top <u>D</u> ata <u>T</u> ools <u>W</u> indow <u>H</u> elp
🎎 Sampling Setup	🗾 🛐 🕨 🕪 🗆 🚳 2K 💌 👫 📶 100KHz 💌 🚥
🚜 Channels Setup .	Sampling Setup
Group into Bus Ungroup from Bus Expand Collapse	Clock Source Asynchronous Clock
Format Row Rename	Synchronous Clock  C External Clock  C External Clock  C Rising Edge Frequency: 100KHz  C Falling Edge (Min:0.001Hz, Max:100MHz)  Note: The external clock voltage level is the same as the port A trigger level
	Sampling       Compression Mode       Signal Filter         RAM Size       2k       Data Compression       Signal Filter         Signal Filter       Signal Filter       Signal Filter         Apply       OK       Cancel       Restore Defaults       Help
-	Fig 4-139 – Compression Mode

**Step4.** Click **Run**, and then activate the signal from the tested circuit to acquire the result on the waveform display area. Fig 4-140 shows the result before and after compression has been applied.





Fig 4-140 – Before and After Compression

Using 128K memory depth, before Compression has been applied, the total of the data was 131072; after the Compression had been applied, the total of the data was 33499998, therefore, the compression rate is 255.585.

Tip: Click 📓 icon to view all data, and then select the waveform analysis tools to analyze the waveforms.

**Step5.** Click the compression icon again or click off the compression function to stop compression.

Tip: Compression cannot be applied with the signal filter function at the same time.



# 4.7 Signal Filter and Filter Delay

The function of the Signal Filter and Filter Delay allow the system to keep the required waveform, and filter out the waveforms that aren't required.

## 4.7.1 Basic Setup of Signal Filter and Filter Delay

Software Basic Setup of Signal Filter and Filter Delay

- Step1. Set up RAM Size, Frequency, Trigger Level and Trigger Position as described in Section 4.1.
- Step2. Set up the trigger edge on the signal or the Bus to be triggered.
- Step3. Click 🙀 icon, or click the Signal Filter Setup from the Sampling Setup dialog box and the Signal Filter Setup dialog box will appear.

		Signal Fil	ter Setup									×
		Filter Con	dition	7	6	5	4	3	2	1	0	
		Post	Trigger Condition	X	X	X	X	X	X	X	х	
		FORTA	Filter Condition	X		X			X			
		PortB	Trigger Condition	$\mathbf{X}$	$\boxtimes$	$\mathbf{X}$	$\mathbf{X}$	$\boxtimes$	$\mathbf{X}$	$\times$	$\times$	
			Filter Condition									
		PortC	Trigger Condition									
LUS LAP-C (16128) (S/I	W:0000000001) = [LaBec1]		Filter Condition									
Bus/Signal Tgigger 1	Sun/Stop Bata Iools Hindow Help	PortD	Trigger Condition									
🔆 Channels Setup .	ampling Setup		Filter Condition									
Group into Bus Ungroup from Bus Expand Collayse Format Row Rename	Clock Source       Annohrmous Clock	Filter Dela V Activ Select O Activ Opp Display Ba V Show Bar 1 Bar 1	y Setup ate Filter Delay Filter Delay Mode cording to Filter Condition posite of Filter Condition r Setup Bari Style Original V width	n		t Delay S Start Edge End Edge Period+De	tart Point		Delay Tim 1 Min: 1) Max: 655	ie:		
	Apply. OK Cancel Restore Defaults Help		ОК			ancel		estore De	faults	ŀ	telp	]

Fig 4-141 – Signal Filter Setup

Set the high level as Filter Condition on the signal A1.

#### Step4. Signal Filter Setup

- 1. Setup the Filter Condition as 📰 or 🖳 on the signal to be analyzed.
- 2. Click **OK**, then click **Run** to activate the signal from the tested circuit to the Logic Analyzer.
- 3. The system will display only the waveforms of the signals which are qualified by the Filter Condition.

Bus/Signal	Trigger	Filter		
🖌 🖌 🔪	z		311. 795us <u>15. 88</u>	30. 525us 20. 4us
🖌 🗚 A1		× -	<u>309. 055us</u>	
🥖 A2 A2				655.36us
🧭 🗚 🕹				655.36us
💉 A4 A4				655. 36us
🖌 A5 A5				655.36us
🖌 🖌 A6		$\boxtimes$		655. 36us
🖋 AT AT	$\boxtimes$	$\boxtimes$		655.36us

Bus/Signal	Trigger	Filter	
AO AO	Z		
🖌 🗚 🗛	- X	-	N 388. 33us
🥖 A2 A2	$\square$		₩ 388. 33us
🧹 A3 A3	$\square$		<u>и</u> 388. 33us
🥖 A4 A4	$\boxtimes$	$\boxtimes$	<u>и</u>
🧪 A5 A5	$\boxtimes$		7 388. 33us
🖌 🖌 A6			<u>и</u>
🖋 AT AT	$\boxtimes$		7 388. 33us

Fig 4-142 – Without/With Signal Filter Setup

The first picture shows the result without any signal filter setup.

The second picture shows the result which has set the high level on the Filter Condition of the signal A1. Only the waveform with the high status of A1 is displayed.

Step5. Filter Delay Setup

- 1. Click on the Activate Filter Delay as shown in Fig 4-143.
- 2. Click on the According to Filter Condition or the Opposite of Filter Condition to select the waveforms to be kept.
- 3. Click on the Start Edge, End Edge or Period + Delay to set the Start Point of Filter Delay.
- 4. Type the value of the Delay Time into the column of the Delay Time.
- 5. Click **OK**, then click **Run** to activate the signal from the tested circuit to the Logic Analyzer.
- 6. The result will be displayed in the waveform display area as shown in Fig 4-142.
- Step6. Stop Signal Filter/ Filter Delay

Technol

Click Stop, then click Signal Filter Setup and select Cancel from the Signal Filter Setup dialog box to stop the Signal Filter or the Filter Delay Setup.

- Tip: Click Stop to check the conditions of the Signal Filter or the Filter Delay Setup, if there aren't any results.
- Tip: Click 📓 icon to view all the data, and then select the waveform analysis tools to analyze the waveforms.



Fig 4-143 - Filter Delay Setup

Tip: Definitions of the Start Edge and the End Edge and the Period + Delay are listed as Figs 4-144, 4-145, 4-146 and 4-147.





















znal Fi	Lter Setup			00	. 40u:	5			20
The Con	distan.								
-Filter Con	aition	7	6	5	4	3	2	1	0
Pointh	Trigger Condition	$\times$	$\times$	$\times$	$\times$	$\times$	$\times$	$\mathbf{X}$	Ţ
TOPCA	Filter Condition								
PortB	Trigger Condition	$\times$	$\times$	$\mathbf{X}$	$\otimes$	$\otimes$	$\times$	$\mathbf{X}$	X
10100	Filter Condition		X				X	X	
PortC	Trigger Condition	$\times$	$\times$	$\boxtimes$	$\otimes$	$\boxtimes$	$\times$	$\otimes$	$\otimes$
10100	Filter Condition								
PortD	Trigger Condition	$\times$	$\times$	$\otimes$	$\otimes$	$\otimes$	$\times$	$\times$	$\otimes$
	Filter Condition								$\square$
Select	vate Filter Delay Filter Delay Mode cording to Filter Condition	n	Selec O s O s	t Delay S Start Edg Ind Edge Period+D	tart Point e elay		Delay Tin 1s (Min:5ns) (Max:327	ne:	
Display Ba	ar Setup								

Fig 4-147 – Filter Delay Setup

The delay time of signal A0 is 1 us, which is the condition of the Filter Delay Setup.

**Step 7.** Signal Filter Time Interval

1. Click Show Bar to know the length of the tested and deleted signal as shown in Fig4-148 below.

Display bar Setup Show bar Bar Style Or Bar Width Sn	iginal 💌	 			
	ОК	Cancel	Restore Def	aults	Help

Fig4-148 - Display Bar Setup

2. The bar has two styles, which are Original and Bar; the default is Original style, which denotes the bar function cannot be used. When selecting Bar style, the bar function can be activated.

- 3. Bar Width, when Bar style is selected, the bar width can be set by users.
- **Tip:** The minimum bar width is 1; the maximum bar width is 65535. If the value exceeds the range, or the font is not according to the requirement, a tip window will appear.



Fig4-149 - Signal Filter Time Interval



Tip: The Signal Filter Time Interval is limited under the following situations.

A: The Filter Delay and Display Bar of Signal Filter are not available under the compression mode.

B: The Filter Delay and Display Bar of Signal Filter are not available under the double mode.

C: The final two data are NULL.

D: Logic Analyzer supports the Signal Filter Time Interval function on condition that the time interval between signal filter must be more than two clocks.



#### **Noise Filter** 4.8

The Noise Filter function enables the system to filter the waveform that doesn't meet users' requirements.

#### 4.8.1 **Basic Software Setup of Noise Filter**

STEP1. Click Data on the Menu Bar, then select 🚾 Noise Filter to activate the noise filter function as the figure below.

Data Tools Mindow Help	
컱 Select an Analytic Range	Noise Filter
nise Filter	
Data Contrast	Noise Filter: None
👪 Find Data Value Ctrl+F	
📮 Find Pulse Width	OK Cancel
14 To the Previous Edge F11	

Fig4-150 - Noise Filter

STEP 2. Transmit the tested signal to the Logic Analyzer as the figure below.



		Fig	94-151 ·	- Tested Signal	
Ρ	3.Filter waveforms	that are not bigge	r than §	5 clocks.	
	Boise Filter				
	Noise Filter:	None 💌		Noise Filter	
	OK	1 clock 2 clock 3 clock		Ause Filter	
	127	4 clock 5 clock 6 clock	l	Noise Filter:	5 clock 🗾 🔻
		7 clock 8 clock 9 clock		ОК	Cancel
		10 clock			

STE

Fig4-152 - The condition of Noise Filter is 5clock.

STEP 4. After filtering the waveforms that are not bigger than 5 clocks, the unqualified waveforms are deleted.

×





Fig4-153 - Waveforms after Filtering

STEP 5. Reserve the original waveform: open the Noise Filter window, and then select None, the waveform will be restored.

Noise Filter 🗙		
Noise Filter:	None 💌	
ОК	1 clock 2 clock	
	3 clock	
127	4 clock	
	5 clock	
	6 clock	
	7 clock	
	8 clock	
	9 clock	
	10 clock	

Fig4-154 - Restore the Waveform



#### 4.9 **Data Contrast**

In order to make users analyze the Data and contrast the difference of Data easily, there are adding the function of Data Contrast. The function of Data Contrast is used to compare the difference of two signal files of the same type. One is the Basic File and the other is the Contrast File. It can line out the different waveform segments of the basic file in the contrast file. Meanwhile, it can count the number of the difference.

#### 4.9.1 **Basic Software Setup of Data Contrast**

STEP 1.Click **Data** on the Menu Bar, then select X to open the Data Contrast Settings dialog box.

	Data Contrast Settings
	Contrast Files Basic File LaDoc1 Contrast File LaDoc1
	Contrast Beginning Point C T Bar C Beginning of Data
	Contrast Result
Data Tools Window Help Select an Analytic Range Noise Filter Data Contrast Find Data Value Ctrl+F	Roll the contrast waveforms synchronization       Pin Assignment         Display files the contrast differences       Perform Contrast         Display files horizontal       OK         OK       Help

Fig4-155 - Data Contrast Interface

Activate Data Contrast: Click the checkbox to activate the function of Data Contrast.

Basic File: It is the standard contrast file.

Contrast File: It is used to compare with the Basic File.

Contrast Beginning Point: It can set the beginning point of the contrast at Trigger Bar or Beginning of Data.

Error Tolerance: It is the allowable time error when setting data contrast.

Contrast Result: It displays the same contrasted result and the different contrasted result with PASS and FAIL respectively.

Error Stat. : It displays the number of discrepant parts.

Pin Assignment: Users can select the contrastive channel.

Perform Contrast: It can activate the Contrast at once.

Display files horizontal: The waveform window of the two contrast files are displayed in horizontal. Users can select it as their requirements and the default is non-activated.

Roll the contrast waveforms synchronization: The two contrast files roll synchronously. Users can select it as their requirements and the default is non-activated.


**Display files the contrast differences:** It can line out the difference in the contrast waveform. Users can select it as their requirements and the default is non-activated.

STEP 2. Display the contrast results in the Data Contrast dialog box.

**Tip**: After pressing Perform Contrast, it will display the contrast information in the contrast result. The below contents of the box are the contrast information. The information is relative simpleness; if users don't want to understand more details, you can know whether the signals of the two contrast files are completely the same or not.

Contrast Files Basic File 00.als		•	
Contrast File 110.als		•	
Contrast Beginning Point T Bar Beginning of Data	Error Toleran	Ce	
Contrast Result		Error Stat.	
A0[A0] FAIL		511	
A1[A1] FAIL		258	
A2[A2] FAIL		129	
A3[A3] FAIL		64	_
A4[A4] FAIL		32	
A5[A5] FAIL		16	
A6[A6] FAIL		8	
A/[A/] FAIL		4	
BU[BU] PASS B1[B1] DASS			Ţ
Roll the contrast waveforms syn Display files the contrast differe Display files horizontal	nchronization nces	Pin Assignmen Perform Contr se Help	ast

Fig4-156 - Display the Contrast Results in the Data Contrast Settings Dialog Box

A0[A0].....FAIL: It indicates that there are differences in the channels of the two files.

B0[B0].....PASS: It indicates that there is no difference in the channels of the two files.

STEP 3. Display the contrast results in the waveform windows. See the figure below.

**Tip**: It contrasts the two data files in the waveform area. The contrast waveform and the basic waveform are displayed horizontally; we can roll the mouse to contrast the waveform files; the difference of the waveforms will be lined out with the red wave line "------" in the contrast files.



Fig4-157 - Display the Contrast Results in the Waveform Windows



# 4.10 Refresh Protocol Analyzer

The Refresh Protocol Analyzer function enables the system to analyze the data between Ds and Dp again.

# 4.10.1 Basic Software Setup of Refresh Protocol Analyzer

STEP 1.Click **Tools** on the Menu Bar, then select 🖄 or click 💁 on the Tool Bar directly to refresh Protocol

Analyzer.

1000 (1000) 1000 (	Customize Show Time of Waveform Co <u>l</u> or Setting
BUS	Bus Property
٠ţ	Refresh Protocol Analyzer
<b>38</b> 3	Memory Analyzer
	Multi-stacked Logic Analyzer Settings
	Analog Waveform

Fig4-158 - Refresh Protocol Analyzer

STEP 2. Transmit the tested Protocol Analyzer signal to the Logic Analyzer, for example Protocol Analyzer SPI.



Fig4-159 - Waveform before Refreshing

STEP 3. Choose Select an Analytic Range to select the analysis range, and drag Ds Bar to B Bar.



Fig4-160 - Drag Ds Bar to B Bar

STEP 4. Click the Logic Analyzer will analyze the data between Ds and Dp.



Fig4-161 - Analyze the Data Between Ds and Dp



STEP 5.Click 🚨	again	, the v	wavefo	orm retu	rn the original	l state.		
Bus/Signal	Trigger	Filter		-20		-5 0	5	
<mark>NewO</mark>	•		UNKNOW	10000000	UNKNOW	10000000	10000000 (	JNKNOW
🖌 AD								
🖌 A1	N							
<b>/ h</b> 2								

Fig4-162 - Restore the Original State

Tip: The Refresh Protocol Analyzer function can come into effect, while the Ds and Dp are activated.



# 4.11 Memory Analyzer

Memory Analyzer enables the system to divide the packet format in the Protocol Analyzer and display the Address and Data in an independent list. It is better for understanding the relative relationship and status of the Address and Data in the operating process of the Protocol Analyzer. Users will know the operation when they use this function. It improves the efficiency of knowing the conditions.

# 4.11.1 Basic Software Setup of Memory Analyzer

STEP 1. Click **Tools** on the Menu Bar, then select **I** to activate the Memory Analyzer function.

🔁 Customize
🐻 Show Time of Waveform
M Color setting
BUS Bus Property
ң Refresh Protocol Analyzer
🚃 Memory Analyzer
📑 Multi-stacked Logic Analyzer Settings
Analog Waveform

Fig4-163 - Memory Analyzer Interface

## STEP 2. Open the Memory Analyzer dialog box

emory Ana	lyzer												×
<< <	>	>> R	eset	Refresh	Merge	Import	Ex	port	Option	Display Alt	eration		
Bus1(IIC)													
Address	Write	data	Read data										
	0	1	2	3	4	5	6	7	8	9	10	11	1
0X0													1
0X10													1
0X20									• Compact r	noae [			1
0X30									Complete	Mode			1
0X40								_					
0X50													
0X60													
0X70													
													-
•												Þ	Г

Fig4-164 - Memory Analyzer Dialog Box

# 1. Compact Mode and Complete Mode:

Click the Right Key in the memory analyzer dialog box; there are two modes for selecting, which are the Compact Mode and the Complete Mode. See the two different figures:

emory And	alyzer	>>   R	eset	Refresh	Merge	Import	Exr	oort	Ontion	Display Alt	eration	2
Bus1(IIC)	 	<u> </u>							- pasterior	[ <u></u>		,
Address	Write d	lata	Read data									
	0	1	2	3	4	5	6	7	8	9	10	11
0X0												
0X10												
0X20												
0X30												
0X40												
0X50												
0X60												
0X70												
4												

Fig 4-165 - Compact Mode

C	emory Ana	alyzer												×
	<< <	>	>> Re	eset	Refresh	Merge	Import	Exp	oort	Option	Display Alt	eration		
	Bus1(IIC)													
		Write	data F	Read data										
	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data	Address	
	OX0		0X1		0X2		0X3		0X4		0X5		0X6	
	0X10		0X11		0X12		0X13		0X14		0X15		0X16	]
	0X20		0X21		0X22		0X23		0X24		0X25		0X26	
	0X30		0X31		0X32		0X33		0X34		0X35		0X36	1
	0X40		0X41		0X42		0X43		0X44		0X45		0X46	]
	0X50		0X51		0X52		0X53		0X54		0X55		0X56	1
	0X60		0X61		0X62		0X63		0X64		0X65		0X66	1
	0X70		0X71		0X72		0X73		0X74		0X75		0X76	
														-
	•													ſ

Fig 4-166 - Complete Mode

# 2. Buttons:

: It is used to find the first packet.

: It is used to find the previous packet.

: It is used to find the next packet.

It is used to find the last packet.

Reset

The data status of each Address will be cleaned out and returned to the original status by

#### pressing the button.

Refresh

: Pressing this button can refresh the data status of each Address data when there are

#### some alterations in the Bus Data

Merge...

: It can merge with the different export files. See the Merge dialog box below.

∎er ge			×
1	2		3
Object file:	C:\\10.txt		Open
File to merge:	C:\\11.txt		Open
		ОК	Cancel

Fig4-167 – Merge Dialog Box

## **Object File:**

1. It is the covered file, that is to say, it is a new file.

2. It can display the path of the "Object File" and the file name.

3. It can open the "Object File" by clicking the "Open" option.

## File to merge:

- 1. It can create the new file with the object file.
- 2. It can display the path of the "File to merge" and the file name.
- 3. It can open the "File to merge" by clicking the "Open" option.



Import...

Export...

: The Export function can select the TXT or EXCEL format to store the

Data of the List Window of the Memory Analyzer; the Import function also can select the TXT or EXCEL formats to analyze the former export data.

Option... : It is used to set the relative parameters for the List Window of the Memory Analyzer; see

the following Option dialog box:

and

Option			<u>×</u>
Bar Assignme	ent		
	Reaction Bar	A	•
Active Displa	y Assignment		
	Display Width	16	•
Color ——			
Addr		Data(R)	
Data(W)		Alteration	
	OK	Cancel	Default

Fig4-168 – Option Dialog Box

**Reaction Bar:** The default is the A Bar; the added Bar can be displayed and selected in the pull-down menu if users have added a new Bar. The data position of the Reaction Bar will be displayed in the List Window of the Memory Analyzer.

Note: The Ds/Dp Bar and T Bar can't be displayed in the pull-down menu.

**Display Width:** It is used to set the display width of the List Window of the Memory Analyzer; the default is 16. Users can select the 4, 8, 16 and 32 from the pull-down menu, and they also can input a value between 1 and 100.

**Color:** Users can vary the color of Addr, Data(R), Data(W) and Alteration as their requirements. The default color of the Addr is black; the default color of the Data(R) is blue; the default color of the Data(W) is red; and the default color of the Alteration is gray.

Display Alteration : The Data in the List Window of the Memory Analyzer will be cleared by pressing this button and the List Window will display the alteration status of each cell. If the same Address has been written or read repetitively, the background of the cell will be gray and the list window will display the Data of the last packet. If the Address doesn't have any alteration, the Address Data will display the data of the Address without the background color. If it is the first time that the Address has been read, we confirm that the data of the packet has been altered.

STEP 3 .Display the Memory Analyzer function in the waveform window.

Tip: The Packet is written; the Address is 0x53; the Data is 0x94, 0xA5, 0xB6, 0xC7, 0xD8 and 0xE9 in



sequence, and the A Bar is the Reaction Bar.







# 4.12 Multi-stacked Logic Analyzer Settings

The function of the Multi-stacked Logic Analyzer Settings is mainly for connecting the hardware of many Logic Analyzers which are the same type, and then use the software to stack the Logic Analyzers which are working independently. It can improve the functions of the Logic Analyzer, which are mainly manifested in two aspects, expanding the RAM Size and adding the number of the test channels.

Tip:

The max. number of the Multi-stacked Logic Analyzers is four. The RAM Size of the four Logic Analyzers can reach to 128K\*4 and the test channels of the four Logic Analyzers can reach to 32\*4. The function of the Multi-stacked Logic Analyzer Settings can be used on LAP-C(32128), LAP-C(321000) and LAP-C(322000).

# 4.12.1 Basic Software Setup of Multi-stacked Logic Analyzer Settings

STEP 1.Click **Tools** on the Menu Bar, then select **i** to activate the function of Multi-stacked Logic Analyzer Settings.

1000 - 10000 - 10000 - 1000 - 1000 - 1000 - 1000 - 1000 - 1000 - 1000 -	Customize Show Time of Waveform Co <u>l</u> or setting
BUS	Bus Property
÷.	Refresh Protocol Analyzer
	Memory Analyzer
	Multi-stacked Logic Analyzer Settings
	Analog Waveform

Fig4-170 - Multi-stacked Logic Analyzer Settings Interface

STEP 2.Click 🧮	to open Multi-stacked Logic Analyzer Settings dialog box
	∎ulti-stacked Logic Analyzer Settings 🛛 🗙
	🔽 Activate Stack
	Stack Type
	C Memory Stack
	• Channel Stack
	Please select the Logic Analyzer for stacking
	□M1 S/N:000000-0000
	_M2_S/N:000000-0000
	_m3_S/1:000000-0000
	Synchronous Channel
	Synchronous Trigger Condition Rising Edge
	OK Cancel Help

Fig4-171 - Multi-stacked Logic Analyzer Settings Dialog Box

Activate Stack: Click the checkbox to activate the function of the Multi-stacked Logic Analyzer; the default is non-activated.

Stack Type: Users can select the Memory Stack and Channel Stack; the default is the Channel Stack.



**Please select the Logic Analyzer for stacking:** It can display all the connected Logic Analyzers and the S/N code of them. The M1 indicates the first Logic Analyzer and the M2 indicates the second Logic Analyzer; M3 and M4 are similar to the previous. Users should select two or more Logic Analyzers, but the most analyzers users can select is four.

**Synchronous Channel:** Select the synchronous channel form the pull-down menu. The default synchronous channel is A0.

**Synchronous Trigger Condition:** Select the synchronous trigger condition. Users can select the Rising Edge, Falling Edge, High and Low from the pull-down menu. The default is the Rising Edge. The function of the Synchronous Trigger Condition can only be used in the Channel Stack, that is to say, it is disabled in the Memory Stack.

STEP 3. Display the function of Multi-stacked Logic Analyzer in the Memory Stack.

**Tip:** There are two Logic Analyzers to do the Memory Stack; the Synchronous Channel is A0; the data on the left of A Bar is captured by the first Logic Analyzer, the data on the right of A Bar is captured by the second Logic Analyzer.

EILS BUSSIE	C (32128)	CS/#:000	000-0000) - [Lo op Esta Iosla	Joc1] Rindow Belg	101 - 101 -	
	16, 12, 1	1 m -		2K + 👬 🚥 10MH	z 🔹 📫 👘 50% 🔹 🐳 Pag	e I · Count I
Scale: 402 2649370 Tetal 89536		h k d	<b>) 🖬 📓 • 🚢</b> ny Fox.16305 nr Fox.0	100% · R 2 8 8	Ls 1. M 1+ +1 3	Height 26 • Trigger 1 A - B = 31730 • Congr-Bate No
Des/Signal	Trigger	Filter	B	. 2151.071 . 11362.001 . 109	ra, 69	11207.619 _ 29638.929 _ 26030.3
AD GTINC)	8	0		16385	Tenden they be deaded to the best	16387
🖌 🔼 45	- III -	10 -	7814		11065	
- / A2 =0	18	0	******		49153	
- C K 🕐	11	8			10155	
M	12	8			49153	
- A5 15	国	0			49153	
100	0.06	-	-		49153	

STEP 4. Display the function of Multi-stacked Logic Analyzer in the Channel Stack.

**Tip:** There are two Logic Analyzers for Channel Stack; the Synchronous Channel is A0; the Synchronous Trigger Condition is the Rising Edge; the former 32 channels (A0~A7, B0~B7, C0~C7, D0~D7) change into the 64 channels (A0~A7, B0~B7, C0~C7, D0~D7, E0~E7, F0~F7, H0~H7, I0~I7) channels.

The street was the	-C (32128)	G/1-00	0000-0000) - [Lafer]]
a tria spesso	are street	er many g	Total farm forme finite former
	14 M	1.2 . 7	-* 25 D DD 2K - # 10MHz + 50% - + Page 1 - Count 1
	<b>1</b> 13	4 8	🕐 🚳 🖷 - 🗶 25% 👻 📽 🔛 🖬 🐮 🛃 14 41 🛐 Berght 18 💌 Trigr
Scals 4 Total 2048		Display ? Trigger ?	Per:0 A Per:-15 + A - T = 15 + A - 3 = 30 + Per:0 B Per:15 + 3 - T = 15 + Compr-Rate Ro
Dus/Signal	Trigger	Filter	-91 -41 -21 -21 -21 -21 -21 -21 -21 -21 -21 -2
AD STER	1		
/ A1 AL 81			
1 A2 12 11			
(A3 83 81			
🖌 🗚 (10.31)			
🖌 A5 👘 ti	C.		
/ A5 A5 E1			
# AT 12 EL			
/ 10 70 H			
/ B1 11 81			
/ R: 12.81			
🧭 B3 🖽 W)			
✓ 34 (34.31)			
✓ 85 10.101			
✓ 16 30 €)			
× 17. 11. 11	1 10	0	
	1 2 .	1 10 1	
EI AL AL			
E = = =			
- C K3 A3 A2			
✓ 24 34.92.			
✓ 85 ±5 ±5			
✓ B = 10			
# ET 17 11			



# **5** Troubleshooting

- 5.1 Installation Troubleshooting
- 5.2 Software Troubleshooting
- 5.3 Hardware Troubleshooting



# Objective

In this chapter, troubleshooting is divided into installation, software and hardware issues. These troubleshooting questions and answers depend not only on our engineers, but also on end users such as students, engineers, technical manual writers, and others.

# 5.1 Installation Troubleshooting

- Q1. Why it is not prompt when I insert the driver CD into my CD-ROM?
- A: At this stage, the driver CD is not auto-executable. The primary issue here is a chipset problem. Though these six Logic Analyzer models seem only different in model number, they are quite different in firmware and chipsets. Due to installation procedures (see *Chapter 2*), we are unable to compile a driver program that auto-detects the chipset at the beginning of the installation.
- Q2. Why does the installation software keep giving an error message saying that I don't have enough memory?
- A: This kind of problem happens in many hardware installations. Turn off multimedia programs such as Media Player, media decoders, media encoders, and so on. If there are any multimedia icons in the system tray (see the far right end of the **START** menu taskbar), remove them. The Logic Analyzer software will run better in memory locations from 64 to 512 MB.
- Q3. What should I do if I want to share this software interface with all users of my computer after installing it?
- A: The shortcut is removing the software interface, and then reinstalling it. By default, the program is available for all users.

## Q4. My HDD is modest; which software components are absolutely necessary?

A: Choose **Custom** as your setup type. Next, unselect items such as examples and tutorials. You must install at least the Main App (application).

## Q5. My MS Windows system will not accept the driver; what should I do?

A: Double check that you run the correct Setup.exe from the folder that corresponds to your hardware and MS Windows version. Visit our website for the latest updated or debugged software. If you are running this program on a virtual machine, the virtual machine may not support the amount of hardware addressing. In this case, try it with a machine that is physically running a Windows system.



# 5.2 Software Troubleshooting

## Q1. Can I run the program even if I don't have the Logic Analyzer hardware?

A: Yes, you can. You can run the program under the demo mode. See. Fig5-1.

ZEROPLUS Logic Analyzer	×
Hardware Searching failed!	
Run Demo Retry Exit	

Fig. 5-1: Select Run Demo if you do not have the actual hardware.

- Q2. I am running a graphing program and software at the same time. Whenever I try to make a screenshot of my work, it keeps telling me that I have insufficient memory space; what is wrong?
- A: A few users have reported similar problems. We are not certain what causes it or how to fix it. However, we have found that if there is a defective address within 128 MB to 512 MB in your physical memory, your software might signal "End of memory". Thus, the program will warn you about insufficient memory. Test your memory with a varied memory testing program. Or, take a screenshot, close the program, paste it to the graphing program, and re-open the program.
- Q3. A part of the background picture remains within the Waveform Display Area, especially when running the program in demo mode. What's wrong with it?
- A: Your machine may have a memory management problem with either your physical RAM onboard or the RAM on your video card. Turn off any other multimedia of graphic programs and then re-run the software. If this does not work, restart your system. This should temporarily fix the problem. However, we highly recommend terminating all irrelevant programs while working with the Logic Analyzer (Try not to burn DVDs, not listen to music or watch movies while working with the Logic Analyzer.).
- Q4. The default color setting of the Waveform Display Area is very cool, but I don't see anything when I print my work out with my black and white laser printer. What can I do?
- A: Refer to Section 3.6; it should have clear, understandable instructions about changing the color of the user interface. See *Fig. 3-153*; this color setting should give a clear view of the Waveform Display Area, even with an old black and white laser printer.



# 5.3 Hardware Troubleshooting

## Q1. Why are no lights on when I hook the USB cable to the Logic Analyzer?

A: Double check whether the other end is properly connected to your PC. There may also be a defect in your USB cable. Try another cable.

## Q2. Why can't I read any signals from my Logic Analyzer?

A: Check whether you have correctly connected the signal cables to the activated pin on your test board and check the power supply of your test board. The Logic Analyzer does not supply any electricity to a test board via signal lines.

#### Q3. I get a signal from only one Logic Analyzer when I have two connected; what is wrong?

A: Currently, only the LAP-C(32128), LAP-C(321000) and LAP-C(322000) support many Logic Analyzers working in series. Also, make sure that the signal lines, power lines, and ground line are properly connected. Refer to Fig. *1-11, Table 1-2, Table 1-3, Table 1-4*, and *Table 1-5*.

#### Q4. Why should I bother grounding? Where can I ground?

A: Grounding will protect the Logic Analyzer and the test board. A proper ground may improve the quality and accuracy of your data. Since it is impossible to avoid unwanted interference you may ground the Logic Analyzer with the test board to ensure that unwanted interference will equally disturb both the testing and tested devices, ensuring a set of data that is still accurate.

# Conclusion

Every user of a product is a potential writer for *Chapters* 5~7 in this User Manual. In fact, this chapter is a composition of many unnamed electronic professionals, especially experts.



6 FAQ

- 6.1 Hardware
- 6.2 Software
- 6.3 Registration
- 6.4 Technical Information
- 6.5 Others



# Objective

In this chapter, common problems and questions are roughly classified into five categories: Hardware, Software, Registration, Technical Information, and Others. This is a backup resource for users, especially those without Internet access. Most references refer to English web links.

# 6.1 Hardware

## H01. Is it ok to substitute stock items for bundled cables and connectors?

A: Yes, users may use any compatible connectors and cables. However, to ensure consistency and accuracy in measurements and data, we strongly recommend using the bundled connectors and cables. Each of the Logic Analyzer's is calibrated with the bundled cables and connectors before packing.

# H02. Does Zeroplus manufacture grippers? How may I purchase grippers?

A: Yes, we have a production line dedicated to grippers. Contact our sales department and a sales representative will be happy to assist you.

## H03. Is the memory size fixed? If I just use one of the ports, can I expand the memory size?

A: The Logic Analyzer's memory is fixed at 4 megabits. Due to current hardware limitations, the memory size cannot be modified, even as the number of ports used changes.

## H04. Are different external sampling frequencies for different channels possible?

- A: No, there is only one external sampling frequency available.
- H05. Can I disable or set a certain port to don't care while during compression?
- A: No, during compression, D Port will be set to be **disabled**.

## H06. Why does the Logic Analyzer feature negative voltage calibration?

A: This allows users to analyze any given signal.

## H07. How do I adjust the Trigger Level?

A: The adjustment of the trigger level is done with a port which consists of 8 channels. The trigger lever can only be adjusted for an entire port.



#### H08. Does the Logic Analyzer use hardware or software compression technology?

A: For time efficiency, the Logic Analyzer uses hardware compression.

#### H09. Is planning an Analyzer that can handle more channels?

A: Yes, we are working in this direction.

#### H10. Does the memory page vary when the depth of the memory changes?

A: Yes, the depth of memory changes the memory page.

#### H11. Is the Logic Analyzer expandable? How may I expand it?

A: Yes, the Logic Analyzer is expandable. At this stage, you can expand it with external module devices.

#### H12. Why must I reinstall the driver every time I use a different Logic Analyzer?

A: Since each Logic Analyzer has unique serial numbers, you must reinstall the driver every time you change the Logic Analyzer.

#### H13. Why is there no data? Why does data sampling seem inconsistent?

- A: The reasons are varied, but you may follow this checklist for troubleshooting:
  - 1) Always check the USB connection between the Logic Analyzer and your PC.
  - 2) We strongly recommend using USB ports in the rear panel of a PC; these ports usually have better voltage stabilities than front panel ports. However, if front panel USB ports are directly soldered to the main board, you can use them.
  - 3) Make sure the Logic Analyzer is directly connected with the PC (without a USB hub).
  - Inconsistent data display may indicate voltage irregularities in the main board; examine capacitors on your main board or power supply.
  - 5) If the problem is the power supply, we strongly recommend purchasing a power supply with a hardwired voltage transformer rather than a voltage regulator. For power supplies with the same output power, those built with hardwired voltage transformers are usually much heavier than those relying on voltage regulators.

#### H14. What are the time settings for "Setup" and "Hold"?

A: Setup Time: 0.05ns ~ 0.25ns; Hold Time: 0.02ns ~ 0.08ns.
 Clock High requires a minimum of 0.31ns. Clock Low requires at least 0.47ns.



# 6.2 Software

#### SW01. Why is the compression function not enabled by default?

A: Mostly to avoid significant errors when testing signals with high variability, or measuring a certain channel for a long time period.

#### SW02. What is the purpose of the compression function?

A: The compression function measures signals that vary slightly over a long period.

#### SW03. Can I enable Trigger Page and Compression Function simultaneously?

A: Yes, you can.

#### SW04. When should I use the "Bar" function?

A: This function allows you to highlight a segment of a waveform so that you can have a closer view. Depending on the configuration of **Waveform Display Mode** under **Tools** → **Customize**, a more accurate numeric value of sampling site, time, or frequency difference will be calculated and displayed as shown in *Fig. 6-1*.



Fig. 6-1 – Bar Function

#### SW05. Can triggers be differentiated in Pre-Trigger and Post-Trigger?

A: Yes, they can.

#### SW06. Are all setup parameters and configurations saved as I save my work?

- A: Yes, everything in your work space, except signal graph, will be saved.
- SW07. If I have the wheel feature with my mouse (or other pointing devices), may I adjust the waveform display zoom, in the Waveform Display Mode by scrolling?
- A: This feature has been enhanced since V1.03. If your program version is prior to this version, visit our website for the latest update at

http://www.zeroplus.com.tw/new\_instrument/main-download.php?type=1

## SW08. What are the extremes for Delay Time and Clock & Trigger Delay Clock?

A: The interface will inform you of the interval you may use. However, it varies from case to case, depending on your test devices. See *Fig.* 6-2.

Delay Time and Clock Trigger Delay Time		
5ns		
(Min:5ns , Max:83.881ms)		
Trigger Delay Clock		
(Min:1, Max:16776191)		

Fig. 6-2 – Delay Time and Clock



#### SW09. How do I know the version number of my software interface program?

- A: Click **Help** from the menu (See Fig 6-3),
  - and then select About ZEROPLUS Logic Analyzer(See Figs 6-3 and 6-4).



Fig. 6-3 - About ZEROPLUS Logic Analyzer



Fig. 6-4 - The circled information is the version number.

#### SW10. How may I upgrade my software interface program?

A: Visit our website at <a href="http://www.zeroplus.com.tw">http://www.zeroplus.com.tw</a> and follow the instructions for the English version. You may also use the following address for English updates. <a href="http://www.zeroplus.com.tw/new">http://www.zeroplus.com.tw</a> http://www.zeroplus.com.tw/new instrument/main-download.php?type=1

#### SW11. Can I save my signal data to a separate pure text file (\*.txt)?

A: This feature is available in this version.

#### SW12. Why is the text display covered by other text or outside the display width?

A: At this stage, our software interface program has missing code for multilingual support. You will have to ensure your system default encoding is one of the following languages: 1) any English Encoding (en, en-XX), 2) Traditional Chinese (zh, zh-XX), 3) Simplified Chinese (zh, zh-CN in HZ, GB2312, GB18030). Double check the language configuration in Region and Language Option.



Fig.6-5 – Windows Regional and Language Options



- SW13. Is there a Reset that restores the default color settings for signal output waveforms in the Position Signal Display Area?
- A: Yes, there is. Click **Tools** from the menu bar, and select **Color Setting**; click **Defaults**. However, this restores everything in this window. You must make a further adjustment if the color setting is the only thing you want to restore. See *Fig. 6-6*.



Fig. 6-6 - Restore Color Defaults

# SW14. Can I change the displayed waveform mode?

- A: Yes, you can. There are two ways to do this.
  - First, go through Data → Waveform Mode and choose a waveform. See Fig. 6-7.



Fig. 6-7 – Waveform Mode

The second alternative is to right-click any place in the Waveform Display Area. Then, a menu will pop up. Click **Waveform Mode**, and choose a waveform. *See Fig. 6-8.* 



问	Find Data Value	Ctrl+F	
<b>–</b>	Find Pulse Width		
	Go To	+	
	Place	•	
<b>+</b> ≧ Ba⊦	Add Bar		
N	Zoom	E	
87	Hand	н	
R	Normal	ESCAPE	
555	Show all Data	F10	
$\mathbb{K} \widehat{}$	Previous Zoom	Ctrl+Z	
	Data Format	•	
	Waveform Mode	•	Reverse
	Color		<ul> <li>Square Waveform</li> </ul>
	Bus Data Color		Sawtooth Waveform
	Bus Single Data Colo	r	

Fig.6-8 – Waveform Mode

# SW15. Can I change the Signal Display Mode into the Timing Mode?

A: Yes, you can.

## SW16. Why does not Filter Delay work when the Double Mode is enabled?

A: To optimize signal output quality and maximize memory efficiency, the **Signal Filter Setup** function may work under the Double Mode. However, the **Filter Delay** function DOES NOT work under the Double Mode at this stage.

# 6.3 Registration

## RG01. What is the significance of the hardware serial number?

A: Every product is assigned and engraved with a unique serial number, which allows us to trace the original manufacturing date of a specific product.

# RG02. How do I register online?

A: Visit our homepage at <a href="http://www.zeroplus.com.tw">http://www.zeroplus.com.tw</a>. Choose the Instrument Department, and click on English. You may also enter the following address: <a href="http://www.zeroplus.com.tw/new\_instrument/main-member-register.php?flag=insert">http://www.zeroplus.com.tw/new\_instrument/main-member-register.php?flag=insert</a> Once you finish membership registration, proceeding with product registration. After finishing product registration, you will receive an email consisting of your product registration information. A password may be required for further customer services and other inquiries.

## RG03. What should I do if online registration fails?

A: Do a screen grab of the window, including the error message, and email our customer service dept. A customer service representative will be glad to assist you as soon as possible once the email is correctly received.

# RG04. How may I register if the purchasing date was more than one month ago?

A: In this case, fill in the registration card and send it via post, fax, or email to our customer service dept, and a representative will process the registration for you.

# RG05. What is the warranty length for my product?

A: A two-year FACTORY WARRANTY is offered in which you will have to send the defective product to the closest branch, an authorized service site, or our headquarters. The in-store warranty may vary, and many require extra charges for various extended warranty policies. The company is not being responsible for an in-store warranty that exceeds our factory warranty.

# RG06. Why should I register this product?

A: If you do not register this product, the warranty will be counted from the manufacturing date indicated by the serial number of your product. Thus, we strongly recommend registering your product for your own benefit.

## RG07. What should I do if the hardware serial number is previously registered?

A: In this case, take a picture of the decal on the rear side of the product and fill in the registration form. Call us and mail both picture and registration to us. A customer representative will be happy to assist you.

# RG08. How do I register the protocol analyzer and buy protocols?

A: Every product is assigned and engraved with a unique serial number. please print your S/N number window as an example attachment and send it to our distributor or ZEROPLUS head office. According to your S/N, we will provide passwords for your protocol registration.

# 6.4 Technical Information

## TI01. What is the Logic Analyzer?

A: The Logic Analyzer is a tool that sieves out and shows the digital signal from test equipment by using a clock pulse. The Logic Analyzer is like a digital oscilloscope. However, it only shows two voltage states (the logic status 1 and 0), differing from many voltage levels of an oscilloscope. The Analyzer has more channels than an oscilloscope to analyze the waveform. Since the Logic Analyzers obtains only signals 1 and 0, its sampling frequency is slower than an oscilloscope, which needs many voltage ranks. Moreover, the Logic Analyzer can receive many signals during a test.

#### TI02. How does the Logic Analyzer operate?

A: The Logic Analyzer reserves trigger requirement setting for users and uses them on the test equipment for the value of the sampling signals and puts them into the internal memory. The software of the Logic Analyzer will read out the value from the memory and switch it to the waveform or status shown for users' analysis.

#### TI03. What is the asynchronous Timing Mode?

A: Since the sampling clock and tested objects are not directly related to each other, and the former won't be controlled by the latter, the sampling clock and the tested signals will not be done at the same time. We call this "Timing Mode", which means that in the same time interval, you can get sampling data from the test equipment at one time, such as every 10 seconds. The internal clock, the Logic Analyzer's inner confirmed one, is often for sampling in Timing Mode as is the logic waveform.

#### TI04. What is the synchronous State Mode?

A: Because the sampling clock and measured object can be directly related, and are controlled by the latter, signals of the former and the latter can proceed simultaneously. We call this "State Mode". In this mode, the measured object provides the sampling clock. State Mode is when the Logic Analyzer can obtain sampling data from the test equipment synchronously. In other words, when the test equipment has a signal or signal group, this is the time to get the signal. For example, while the test equipment is sending out one rising edge, the Logic Analyzer can start to obtain one signal.

## TI05. What are A-bar, B-bar and T-bar?

A: The T-bar, A-bar and B-bar are labels. T is the trigger label, which cannot be removed when the waveform or the state is displayed, which marks a pod. When searching for, or obtaining data, the A and B labels can be set in any location. Using the order of these markings, you can return quickly to the desired position to analyze data. This can also be a point to measure the interval between A-B, A-T, or B-T.

#### TI06. What is a Trigger Gripper?

**A:** A gripper is the gathering point to collect the Logic Analyzer channels. When a cable connector is not suitable for the test device, a trigger gripper may be an alternative for connection.

## TI07. What is a Channel?

A: The channel is the collection line of the input signal. Each channel is responsible for linking the pin of the measured device. Every channel is used to collect signals from the test equipment.

#### TI08. How can I display acquisition in the waveform captured by external sampling signal?

A: Select Waveform Display from the Window list.

#### TI09. What is an External Trigger?

A: An external trigger is a signal outside the Logic Analyzer. It is used for the simultaneous test of 2 test tools. For example, one Logic Analyzer can be started by one signal from another test tool. Or when it is triggered, it can output one signal to another test tool. The Logic Analyzer is often used for triggering an oscilloscope.

## TI10. Why does Double Mode not coincide with Filter Delay?

A: In order to set out the perfect waveform from the Logic Analyzer and achieve optimal memory efficiency, you can use the **Signal Filter** when using **Double Mode**; the system doesn't support the function of **Filter Delay**.

## TI11. How do I update software?

A: The software will automatically check for and download updates. This function deletes old software first and



then downloads and installs the latest version.



## OT01. How was the Logic Analyzer developed?

A: It took us more than two years to develop this product. We envision "Everyone carrying the Logic Analyzer," and we would like to make some contributions to the electronics industry in return. We also wish to transform the stereotypical OEM factory into a world class R&D center.

## OT02. Why is there a rich information database for game chips rather than the Logic Analyzer?

A: First of all, we apologize for any inconvenience caused by the lack of information pertaining to Logic Analyzers. We are currently working very hard on multilingual information and documentations pertaining to the Logic Analyzer. Visit our website for the latest drivers, software, and manuals: <a href="http://www.zeroplus.com.tw/new\_instrument/index.php?lang=eng">http://www.zeroplus.com.tw/new\_instrument/index.php?lang=eng</a>. In the meantime, we will have updates ready when verified error free.

# OT03. What was the original intention of developing this item?

A: Originally, the Logic Analyzer was just for use by our engineering department. Later on, we saw the greater need for this kind of device. We made numerous enhancements and made it available to the public.

# Conclusion

This chapter is full of hard facts for engineers. The contents of this version of the User Manual may look more different than the one on the web. Every engineer finds new problems, new solutions, or other issues, during real life applications. Though there are dozens of questions here, we look forward to your feedback, which is important for future versions. It may help us produce more efficient and accurate devices so that we will offer you much better service.



# 7 Appendix

- 7.1 Hot Keys
- 7.2 Contact Us



# Objective

In this chapter, users will learn the functions of all defined hot keys in the software interface of the Logic Analyzer.

Hot Key	Equivalent Orders	Statement
А	Go to A Bar	Move the A-bar to the center of the waveform area; select A-bar by the cursor.
В	Go to B Bar	Move the B-bar to the center of the waveform area; select B-bar by the cursor.
Т	Go to T Bar	Move the T-bar to the center of the waveform area; select T-bar by the cursor.
E	Change to Zoom mode	Change the mouse mode to Zoom
Н	Change to Hand mode	Change the mouse mode to Hand.

# 7.1 Hot Keys

# Table 7-1: Hot Keys (1)

# Table 7-2 : Hot Keys (2)

Hot Key	Equivalent Orders	Statement
Ctrl + A	Go to A Bar	Center A-bar.
Ctrl + B	Go to B Bar	Center B-bar.
Ctrl + C	File -> Capture Window	Open Capture Graph dialog box.
Ctrl + E	Data ->Zoom	Change Mouse mode to Zoom mode.
Ctrl + F	Data -> Find Data Value	Search specific data with predetermined conditions.
Ctrl + G	Bus/Signal -> Group into Bus	Group selected signals into a Bus.
Ctrl + N	File -> New	Create a new file.
Ctrl + O	File -> Open	Open a saved file.
Ctrl + P	File -> Print	Print an active file.
Ctrl + S	File-> Save	Save an active file with its current name, location and file format.
Ctrl + U	Bus/Signal -> Ungroup from Bus	Ungroup signals (Pins) from a Bus.
Ctrl + Z	Data -> Previous Zoom	Reverse the last zoom.
Ctrl + Shift + E	File->Export Waveform	Open Export Waveform dialog box.



# Table 7-3 : Hot Keys (3)

Hot Key	Equivalent Orders	Statement
Page Down	Operate the position shown	Go to next page of the data or the waveform
Page Up	Operate the position shown	Go to previous page of the data or the waveform
Home	Operate the position shown	Go to the beginning of the data or the waveform
End	Operate the position shown	Go to the end of the data or the waveform.
Up	Operate the position shown	Move the cursor up a grid.
Down	Operate the position shown	Move the cursor down a grid.
Left	Operate the position shown	Move the selected Bar or display left to prior the waveform or data.
Right	Operate the position shown	Move the selected Bar or display right to posterior the waveform or data.
ESC	Operate the position shown	Release all selected bars, and change Mouse mode to Normal.
Space	Change the trigger conditions	Change trigger conditions.

# Table 7-4 : Hot Keys (4)

Hot Key	Equivalent Orders	Statement
F1	Help -> Logic Analyzer Help	Logic Analyzer Help
F2	Decrease the sampling rate	Decrease the sampling rate
F3	Increase the sampling rate	Increase sampling rate
F5	Run/Stop -> Single Run	Execute the acquirement once
F6	Run/Stop -> Repetitive Run	Execute the acquirement continuously
F7	Run/Stop -> Stop	Stop acquiring data
F8	Data -> Zoom Out	Zoom out the waveform
F9	Data -> Zoom In	Zoom in the waveform
F11	Data ->To the Previous Edge	Move forward to the prior variation waveform and center that location.
F12	Data -> To the Next Edge	Move forward to the next variation waveform and center that location.





# 7.2 Contact Us

Table 7-5: Contact Us

Contact Us			
Copyright 1997-2009, ZEROPLUS TECHNOLOGY CO., LTD			
Headquarter			
Taiwan-Chung Ho City	ZEROLUS TECHNOLOGY CO., LTD. 3F., No.121, Jian Ba Rd., Chung Ho City, Taipei County, R.O.C. Tel: +886-2-6620-2225 Fax: +886-2-6620-2226 ZIP Code: 23585		
Instrument Division/			
Business Department			
Taiwan-Hsinchu City	ZEROLUS TECHNOLOGY CO., LTD. 6F., No.265, Wuling Rd., North District, Hsinchu City, Taiwan (R.O.C.) Tel: +886-3-542-6637 Ext.:87 Fax :+886-3-542-4917 Service E-mail: <u>service 2@zeroplus.com.tw</u>		
Taiwan-Chung Ho City	ZEROLUS TECHNOLOGY CO., LTD. Address: 2F, NO.123, Jian Ba Rd, Chung Ho City, Taipei Hsian, R.O.C. Tel: 886-2-6620-2225 Ext.:200 Fax: 886-2-6620-2226		
Other Service Departments			
China-Shenzhen	ZEROPLUS TECHNOLOGY (DONG GUAN) CO., LTD. Room 2821, B2 Section, Building 1, Hong Rong Square, District 80, Bao'an, Shenzhen City, Guangdong Province, China Mainland Tel: +86-755-2955-6305~6 Fax: +86-755-2955-6306 #808 ZIP Code: 518102		
China-Shanghai	ZEROPLUS TECHNOLOGY (DONG GUAN) CO., LTD. 101, No. 172, Alley 377, Chen Hui Road, Zhang Jiang, Pudong New Area, Shanghai City Tel: +86-21-50278005~6 Fax::+86-21-50278006 ZIP Code: 201203		

Users can download the newest Software and User Manual.

ZEROPLUS is the brand of ZEROPLUS TECHNOLOGY CO., LTD.

The other brands and products are the brand or registered trade mark of the individual company or organization.



# Conclusion

The demonstrations in this User Manual will enhance users' understanding of our products in future issues, even though the manual ends here. We thank you for choosing the Logic Analyzer. Please contact us if you find anything that could be done better, either in software or hardware. We appreciate your feedback.